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VOLUME 241

Low Temperature (LT) GaAs and Related Materials

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VOLUME 241

Low Temperature (LT) GaAs and Related Materials

EDITORS

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Preface

The first meeting for this young, rapidly evolving topic was an invitational workshop held in association with the Spring 1990 MRS Meeting. Prior to that event, no more than one or two papers on the topic had been presented at the same meeting or published in the same journal issue. The response to this symposium, less than two years later, accurately reflects the increasing awareness of the rich combination of fundamental materials science and electronic/optoelectronic applications that are at play in the subject.

The gradual and incomplete understanding of the basic mechanisms responsible for the remarkable properties of these materials have produced a confusion of names. At the time of planning for this symposium the organizers attempted to select a suitable name, one reflecting the understanding to date. However, events would have it otherwise. The then common phrase "low temperature" or "LT" GaAs was adopted reluctantly. In doing so, it was realized that this phrase is misleading and inaccurate. More appropriate are two other phrases used in these proceedings: GaAs with arsenic precipitates or GaAs:As and low temperature grown or LTG GaAs. This issue of terminology remains to be resolved.

More basic issues than terminology continue as challenges. The most important of these is the understanding of the roles played by deep level defects (found in unprecedented concentrations in as-grown material) and arsenic precipitates (noted primarily in annealed samples). This issue sparked lively discussions in the symposium. The presentation in these proceedings of the two main points of view on this matter is handicapped by the absence of two key papers read at the meeting. However, the papers in Parts I and II provide a good background and list the key references.

The potential for electronic and optoelectronic applications of LTG GaAs is made apparent by the papers in Part III. An excellent introduction is provided by the Overview paper by Frank Smith, one of the originators of this subject. It is interesting that at least one company has incorporated LTG GaAs buffer layers in commercial products at this early stage of understanding.

The last set of papers, in Part IV, introduce an extension of low temperature growth to ternary compounds, such as InGaAs and AlGaAs, and to the InP-based family. The ternaries studied share, with exceptions, many of the properties of LTG GaAs. Four groups report on the first efforts to use LTG techniques to produce highly resistive InP layers.

G.L. Witt
A.R. Calawa
U.K. Mishra
E.R. Weber

March, 1992

Acknowledgments

Thanks are due to the contributors and participants in this symposium. The quality of the contributed papers was high, the attendance was all that had been anticipated, and the discussions were spirited. A special salute is extended to the invited speakers whose presentations effectively set the background and tone for the entire symposium. They were:

A.R. Calawa	F.W. Smith
Z. Liliental-Weber	E.R. Weber
U.K. Mishra	J.M. Woodall
G. Mourou	

In a discussion-intensive meeting such as this, session chairs played a key role. In addition, they had major responsibility for the refereeing of the manuscripts. They were:

M. Delany	F.W. Smith
C. Kocot	E.R. Weber
D.C. Look	G.L. Witt
W. Schaff	

The entire MRS staff was most cooperative in providing support when required, often without being asked.

The editor recognizes the major contributions of his fellow committee members, whose efforts made this symposium not just possible but an outstanding success. They are:

A.R. Calawa
Massachusetts Institute of Technology, Lincoln Laboratory

U.K. Mishra
University of California at Santa Barbara

E.R. Weber
University of California at Berkeley

G.L. Witt, Editor
March 1992

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Overview

DEVICE APPLICATIONS OF LOW-TEMPERATURE-GROWN GaAs

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ABSTRACT

Low-temperature-grown (LTG) GaAs is a unique material that has been used in a variety of device applications to achieve record performance. LTG GaAs used as a buffer layer eliminates sidgating and backgating and in GaAs integrated circuits. Record output power density (1.57 W/mm) and superior microwave-switch performance were demonstrated when LTG GaAs was used as a gate insulator in a metal-insulator-semiconductor field-effect transistor. High-speed (0.5 ps) and high-voltage (1 kV) LTG GaAs photoconductive switches have also been demonstrated. Using the same material, researchers have demonstrated high-responsivity (0.1 A/W), wide-bandwidth (~ 375 GHz) LTG GaAs photodetectors.

Devices incorporating LTG GaAs are currently being optimized for systems applications. LTG GaAs technology can enhance system performance and enable new systems for military and commercial applications in the areas of radar, communications, instrumentation, and high-speed computing.

INTRODUCTION

Low-temperature-grown (LTG) GaAs was discovered at Lincoln Laboratory by A. R. Calawa in the mid 1980's and has been applied to electronic and photoconductive devices and circuits since that time. LTG GaAs is deposited by molecular beam epitaxy (MBE) at relatively low substrate temperature (~ 200°C). Some of the unique features of LTG GaAs are contrasted with conventional GaAs grown by MBE in Table 1. Most importantly for device applications, the large excess As concentration in LTG GaAs results in a large trap density, that in turn results in a high resistivity, a large breakdown field, and an extremely short photoexcited carrier lifetime.

Record device and circuit performance achieved using LTG III-V semiconductors has made it clear that this new materials system has a number of unique and desirable properties. LTG III-V materials that have been demonstrated include LTG GaAs, AlGaAs, InAlAs, InGaAs, and InP. Of these materials, the one most extensively characterized and utilized in

Table 1 Comparison of the properties of LTG GaAs with undoped GaAs grown by MBE.

	MBE GaAs	LTG GaAs
GROWTH TEMPERATURE	600°C	200°C
STOICHIOMETRY	STOICHIOMETRIC GaAs	1 at. % EXCESS As $\text{Ga}_{0.495}\text{As}_{0.505}$
TRAP DENSITY	$< 10^{15} \text{ cm}^{-3}$	$\sim 10^{19} \text{ cm}^{-3}$
BREAKDOWN FIELD	$\sim 3 \times 10^4 \text{ V/cm}$	$\sim 5 \times 10^5 \text{ V/cm}$
RESISTIVITY	$0.3\text{-}20 \Omega \cdot \text{cm}$	$\sim 10^6 \Omega \cdot \text{cm}$
PHOTO-EXCITED CARRIER LIFETIME	$\sim 1 \text{ ns}$	150 fs

device and circuit applications is LTG GaAs. For this reason, this paper will exclusively address LTG GaAs, although other papers in this volume will address the properties and applications of other LTG III-V materials.

LTG GaAs has been exploited in electronic devices, photoconductive devices, and integrated circuits (ICs). LTG GaAs used as a buffer layer has eliminated sidegating and backgating in GaAs ICs and has been shown to reduce short-channel effects in GaAs field effect transistors (FETs) [1]-[4]. When used as a gate-insulating layer, LTG-GaAs-based metal-insulator-semiconductor field-effect-transistors (MISFETs) have achieved record output power density [5]-[6]. Record bandwidth and responsivity have been reported from an LTG-GaAs photodetector [7].

In this paper, a brief summary of the properties of LTG GaAs will be given, followed by a more detailed discussion of the device applications. Lastly, some of the potential systems applications of LTG-GaAs-based components will be presented.

PROPERTIES OF LTG GaAs

Other than the growth temperature, the MBE growth parameters for LTG GaAs are those typically used for conducting GaAs layers. The growth rate is $\sim 1 \mu\text{m/h}$ on (100)-oriented GaAs substrates. As the growth temperature for GaAs in MBE is reduced from the standard 500-600°C range (with post-growth annealing temperature maintained at 600°C), the resistivity of the annealed LTG GaAs increases, though the layer remains crystalline for growth temperatures as low as 150°C. LTG GaAs appears to be stable at elevated temperatures, and high-quality conducting GaAs can be grown on it at normal growth temperatures. After annealing, the material has high resistivity ($> 10^6 \Omega \text{ cm}$), short photoexcited carrier lifetime ($\sim 150 \text{ fs}$), relatively large photoexcited carrier mobility ($\sim 200 \text{ cm}^2/\text{V s}$), and large breakdown field ($\sim 5 \times 10^5 \text{ V/cm}$).

LTG GaAs has been extensively characterized. A tentative semiquantitative model of annealed LTG GaAs has been formulated using these results and is shown in Fig. 1 [8]. As-grown LTG GaAs displays a dilated lattice constant, has approximately 1 at. % excess arsenic, and contains $\sim 10^{20} \text{ cm}^{-3}$ As_{Ga} -related defects of which $\sim 5 \times 10^{18} \text{ cm}^{-3}$ are ionized. An isolated V_{Ga} or V_{As} complex is hypothesized to be the compensating acceptor. LTG GaAs layers are crystalline only up to a certain temperature-dependent thickness, after which the layer becomes polycrystalline [8]. At 200°C, the growth temperature we typically use, crystallinity is maintained for thicknesses up to $\sim 3 \mu\text{m}$.

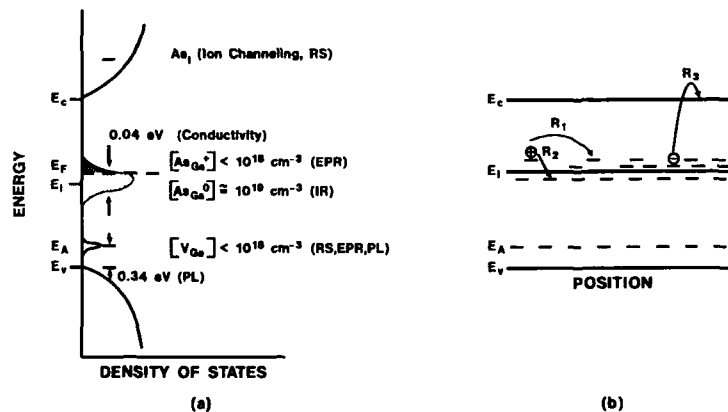


Figure 1 Preliminary model for 200°C LTG GaAs annealed at 600°C for 10 min. (a) Density of states and (b) band diagram. The techniques used to identify the defects in (a) are shown in parentheses. R_1 , R_2 , and R_3 in (b) refer to the three conduction mechanisms that occur in LTG GaAs, nearest-neighbor hopping, variable-range hopping, and free-electron conduction, respectively.

The deep-level density and disorder in LTG GaAs are observed to decrease monotonically with post-growth annealing temperature. However, the ~ 1 at. % arsenic excess in the crystal is unchanged by an *in situ* anneal with an As overpressure. The V_{Ga} and As_{Ga}^{+} -related defects are reduced below detectable levels by the anneal, although As_{Ga} -related defects remain, and As microprecipitates are formed [8]. We attribute the large breakdown fields to an extremely large trap-filled limit voltage, arising from the large deep-level density in the material. As is the case for the as-grown material, the annealed LTG GaAs shows quenched photoluminescence, strong deep-level infrared absorption, and hopping conductivity at low temperature.

An alternative model to explain the electrical and optical properties of LTG GaAs has been proposed by researchers at IBM and Purdue University and is based on the presence of As precipitates in the annealed material [9]. This model is discussed in detail in the paper by Warren and Woodall in this volume. Whether the deep-level model or the As-precipitate model is the correct one for annealed LTG GaAs is still an open question.

LTG GaAs BUFFER

A number of problems associated with GaAs-based metal-semiconductor field-effect transistor (MESFET) and high-electron-mobility transistor (HEMT) devices and circuits are attributed to the semi-insulating GaAs substrate. Such problems include sidegating (or backgating), hysteresis in the dependence of the drain-source current I_{DS} upon drain-source voltage V_{DS} , light sensitivity, low output resistance R_o , low source-drain breakdown voltage BV_{SD} , and low output power gain at RF frequencies [10]-[12]. In addition, increased subthreshold leakage current, shifts in threshold voltage, and inability to fully pinch off the device for large V_{DS} can occur as the gatelength of GaAs-based MESFETs and HEMTs is reduced to submicrometer dimensions [13]-[15].

To alleviate these effects, a buffer layer is often inserted between the active layer and the substrate. A number of buffer layers are currently in use by GaAs IC manufacturers, including undoped GaAs, AlGaAs, and superlattice (AlGaAs/GaAs) buffers. However, these buffer layers have resulted in only limited success in mitigating the problems outlined above. In contrast, the LTG GaAs buffer layer has been shown to eliminate sidegating in MESFETs [1] and HEMTs [16] and to dramatically reduce short-channel effects in submicrometer-gatelength MESFETs [2].

Sidegating Elimination

Sidegating is the reduction in I_{DS} of a MESFET or HEMT as a result of a voltage applied to an adjacent and nominally isolated device. For IC applications, the restrictions on device and circuit layout currently imposed by the sidegating effect can be eliminated by using the LTG GaAs buffer. In our first publications in this area [1], [2], we showed that an LTG GaAs buffer eliminates dc sidegating effects in GaAs MESFETs. Selected results of our experiments are shown in Fig. 2. We compared MESFETs fabricated upon the LTG GaAs buffer, MESFETs fabricated upon other buffer layers, and MESFETs formed by direct implantation into a semi-insulating substrate. We found that only the LTG GaAs buffer eliminates dc sidegating under both dark and white-light conditions throughout the MILSPEC temperature range. We also found that the LTG GaAs buffer significantly increased R_o and BV_{SD} for these 2- μ m-gatelength MESFETs, as compared with the other buffer layers. As shown in Fig. 2, superlattice buffers are superior to undoped buffers, but they do not eliminate sidegating in MESFET and HEMT ICs, even for relatively low voltages (10 V) across relatively large spacings (50 μ m).

The LTG GaAs buffer has also been shown to markedly reduce the coupling of pulse trains and RF signals between devices, which is an important consideration for both analog and digital ICs [4]. Thus, the LTG GaAs buffer should provide much better isolation between digital control signals and the active devices in monolithic microwave ICs (MMICs).

Hewlett Packard has applied the LTG GaAs buffer to their HEMT and MESFET MMICs and have found that sidegating effects and light sensitivity are eliminated. They showed that no sidegating in HEMT MMICs was observed even for 70 V applied across a 3- μ m spacing [16]. In fact, they found that dielectric breakdown occurs in their structures before sidegating is observed. Hewlett Packard has performed extensive reliability tests on LTG GaAs and has found that the material meets their stability criteria for use in products [17].

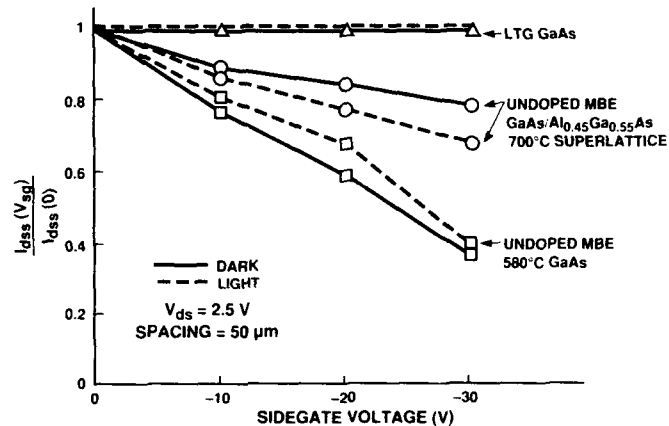


Figure 2 Sidegating characteristics: LTG GaAs buffer, undoped GaAs buffer, and undoped superlattice buffer. The points connected by the solid lines are the results obtained in the dark and the points connected by the dashed lines in the light. The lines themselves are included only as a convenience in visualizing the data.

Devices Fabricated on LTG GaAs Buffers

The LTG GaAs buffer has been shown to substantially reduce short-channel effects in a 0.27- μm -gate-length MESFET [2]. The I_{DS} - V_{DS} characteristics are shown in Fig. 3 for two types of MESFETs, one having a LTG GaAs buffer and one having a standard undoped GaAs buffer. The MESFET fabricated on the undoped buffer layer shows a low R_0 near pinch-off and poor pinch-off for large V_{DS} . In contrast, the MESFET with the LTG GaAs buffer has a large R_0 near pinch-off and pinches off well, even for V_{DS} in excess of 10 V. Selected dc results for these MESFETs are summarized in Table 2. Although the peak transconductance g_m is slightly lower for the MESFET with the LTG GaAs buffer, R_0 is 50 times larger near pinch-off, and BV_{SD} (as measured with the device biased to pinch-off) is two times larger. The values of the maximum frequency of oscillation f_{max} and unity current-gain frequency f_T calculated from the measured scattering parameters are shown in Table 3. These results were measured for $V_{DS} = 2$ V and did not change appreciably for V_{DS} up to 6 V.

Hughes has demonstrated 0.2- μm -gate-length MESFETs fabricated on the LTG GaAs buffer that have g_m values of 600 mS/mm and an extrapolated f_T of 80 GHz [18]. Frequency dividers designed using source-coupled FET logic were fabricated with these transistors and exhibited a clock rate of 22 GHz [18]. This result is among the best ever reported for a frequency divider based on GaAs MESFETs. The device and circuit results obtained using the LTG GaAs buffer clearly indicate that high-quality devices can be fabricated on LTG GaAs buffers.

LTG GaAs MISFET

The LTG GaAs MISFET holds substantial promise for MMICs such as power amplifiers, switches, phase shifters, and attenuators. A LTG GaAs MISFET with a gate length of 1.5 μm delivered an output power density of 1.57 W/mm with 4.4 dB gain and a power-added efficiency of 27.3% at 1.1 GHz [5],[6]. This is the highest power density from a GaAs-based FET ever reported. The LTG GaAs MISFET has also demonstrated switch performance at 1.3 GHz that is comparable to that of the best commercially available FET switches that we have tested.

The epitaxial layer structure of the MISFET is shown in Fig. 4. The devices used in this study were simple microwave FETs with a gate length of 1.5 μm , gate width of 600 μm , and source-drain spacing of 6 μm . In this device, the gate metal was Ti/Au and was deposited directly on the upper LTG GaAs surface without a gate-recess etch. The upper LTG GaAs layer not only forms the gate insulator but also passivates the surface of the device.

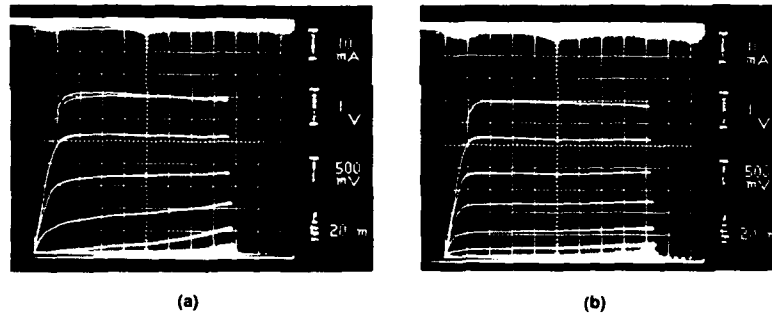


Figure 3 0.27- μm -gate-length MESFET $I_{\text{DS}}\text{-}V_{\text{DS}}$ characteristic: (a) undoped GaAs buffer, and (b) LTG GaAs buffer.

Table 2 Summary of dc results: 0.27- μm -gate-length MESFET.

PROPERTIES	UNDOPED MBE GaAs BUFFER	LTG GaAs BUFFER
g_m (mS/mm)	205	190
R_o (Ω)	1,000	50,000
BV_{DS} (V)	7	14
BV_{ISO} (V)	30	400

Table 3 Summary of RF results: 0.27- μm -gate-length MESFET.

PROPERTIES	UNDOPED MBE GaAs BUFFER	LTG GaAs BUFFER
MAXIMUM STABLE GAIN AT 26 GHz (dB)	10.4	12.0
f_T (GHz)	26	28
f_{max} (GHz)	80	91

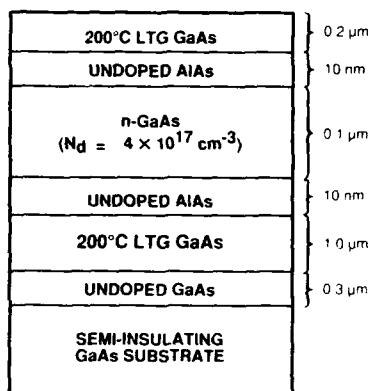


Figure 4 Schematic cross section of the epitaxial layer structure of the LTG GaAs MISFET.

The gate forward turn-on and reverse-breakdown voltages for the MISFET are ~ 9 and 42 V, respectively, as shown in Figs. 5(a) and 5(b). Values of these voltages for our GaAs MESFETs without the LTG GaAs gate insulator are approximately 0.6 and 15 V, respectively. The substantial improvement is attributed to the LTG GaAs gate insulator and passivation. BV_{SD} at pinch-off for the LTG GaAs MISFET is 43 V, as shown in Fig. 5(c). This contrasts with a value of ~ 10 V for our conventional GaAs MESFET. This improvement is attributed to the LTG GaAs buffer and gate-insulator layers.

The drain-source current density of the LTG GaAs MISFET reaches 750 mA/mm at $V_{DS} = 4$ V and gate-source bias $V_{GS} = 2$ V. This density is approximately a factor of two larger than that typically used in GaAs power MESFETs. The high drain current coupled with the large breakdown voltages lead to the high output power density. The f_T and f_{max} of the MISFET at $V_{GS} = -2$ V and $V_{DS} = 4$ V are 8.5 and 14 GHz, respectively. These values are similar to those of our conventional GaAs MESFETs fabricated with the same mask set.

The MIS structure results in a gate capacitance C_G that is lower and more linear with bias than for a MESFET of similar geometry and doping density. The combination of low C_G , low channel resistance, and high breakdown voltages that can be achieved with the LTG GaAs MISFET make it a strong candidate for microwave switching applications. A switch using the LTG GaAs MISFET operating at 1.3 GHz had an on resistance of 3.4 W at $V_{GS} = 1$ V and a drain-source capacitance of 0.4 pF at pinch-off. A figure of merit for a switch, defined as the product of the on resistance and the off capacitance is already better for the MISFET than that obtained with the best commercial MESFETs that we have tested. Furthermore, because of the low gate-leakage current and the high breakdown voltages, the LTG GaAs MISFET can handle higher power than typical GaAs MESFET-based switches. By reducing the on resistance and the off capacitance we should be able to achieve further improvements in switch performance.

LTG GaAs PHOTOCONDUCTIVE SWITCH AND DETECTOR

LTG GaAs is observed to have a significantly lower photoexcited carrier lifetime than GaAs grown at normal substrate temperatures. Using femtosecond time-resolved-reflectance techniques, we have measured a subpicosecond ($\sim 150 \text{ fs}$) carrier lifetime for LTG GaAs grown at $\sim 195^\circ\text{C}$ and annealed at 600°C [19]. As shown in Fig. 6, electrical pulses having full widths at half-maximum (FWHM) less than 0.5 ps have been generated by using LTG GaAs photoconductive switches having a $20\text{-}\mu\text{m}$ gap between conductors [19]. Good responsivity for a photoconductive switch is also observed, corresponding to a mobility of the photoexcited carriers of $\sim 200 \text{ cm}^2/\text{V s}$. The combination of fast recombination lifetime, high carrier mobility, and high resistivity makes LTG GaAs ideal for a number of subpicosecond photoconductive switch applications.

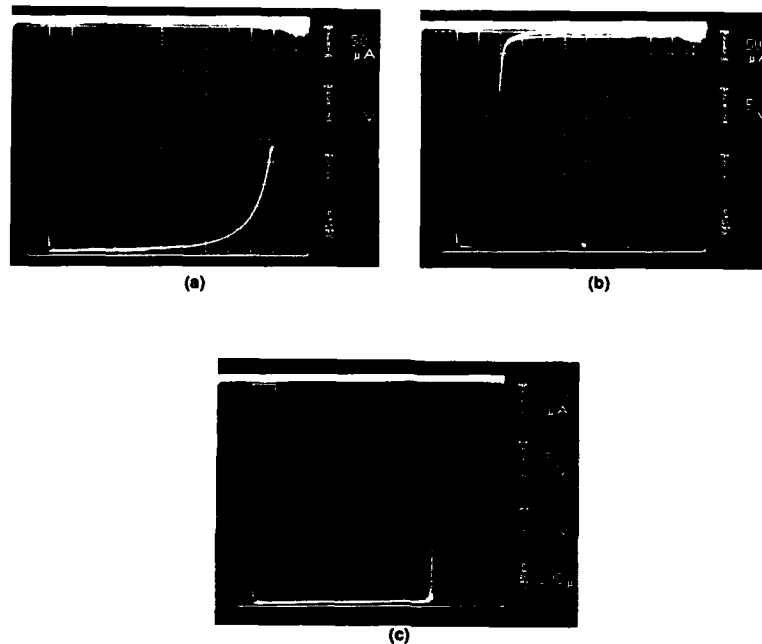


Figure 5 The (a) forward and (b) reverse gate characteristics of the LTG GaAs MISFET. (c) The I_{DS} - V_{DS} characteristics of the LTG GaAs MISFET for $V_{GS} = -8$ V (pinch-off).

Figure 6 also shows recent work in which researchers at the University of Michigan have demonstrated the generation of ~ 1 kV electrical pulses having FWHM values of less than 3 ps using an LTG GaAs photoconductive switch having a 60- μ m gap [20]. This is the largest voltage ever switched at picosecond speeds. Applications for such pulses include millimeter-wave radar, switched power supplies, and ultrafast instrumentation.

Researchers at the University of Michigan have also developed a new metal-semiconductor-metal photoconductive detector based on LTG GaAs with a response time of 1.2 ps and a responsivity of 0.1 A/W. To our knowledge, this is the fastest high-sensitivity photoconductive detector of any kind reported to date. This detector was fabricated using interdigitated electrodes spaced 0.2 μ m apart [7]. In addition, the device can be driven to an on-state resistance of 30 Ω with little degradation in speed. This versatility permits the device to function both as a detector and a switch. Such unique dual functionality together with an ease of integration with GaAs ICs will permit a number of detector elements to be combined on an IC for acquiring and processing high-speed optical and electrical events.

LTG GaAs SYSTEMS APPLICATIONS

As a result of the successes that have been obtained by researchers using LTG GaAs and other LTG III-V materials in electronic and photoconductive applications, a number of systems applications for these materials are possible. Figure 7 schematically summarizes a few of the device applications and systems applications of LTG III-V materials.

MISFETs, MESFETs, and HEMTs fabricated using LTG GaAs can be used as microwave power amplifiers and control circuits. The pulses generated using the LTG GaAs photoconductive switch can be radiated into free space and used as high-power, wide-bandwidth sources for the millimeter and submillimeter wavelength ranges. Alternatively, LTG

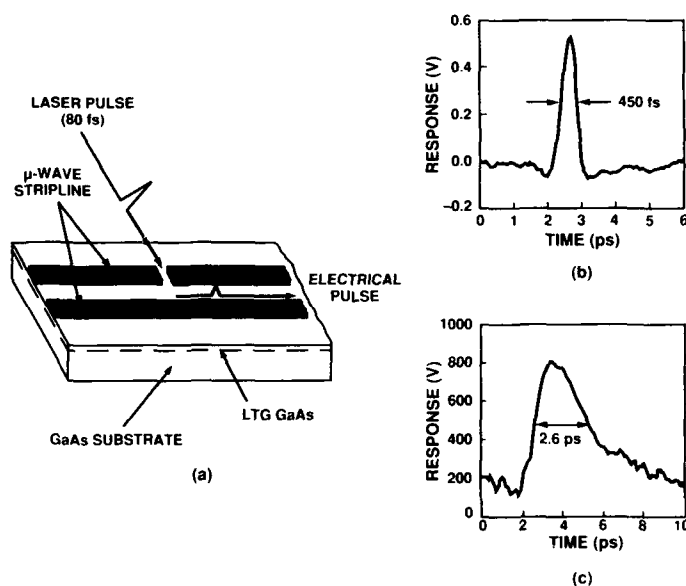


Figure 6 Summary of the LTG GaAs photoconductive switch: (a) perspective view of the photoconductive-gap switch, (b) subpicosecond electrical pulse for a 20- μ m gap and a 10-V bias, and (c) high voltage electrical pulse for a 60- μ m gap and a 700-V bias.

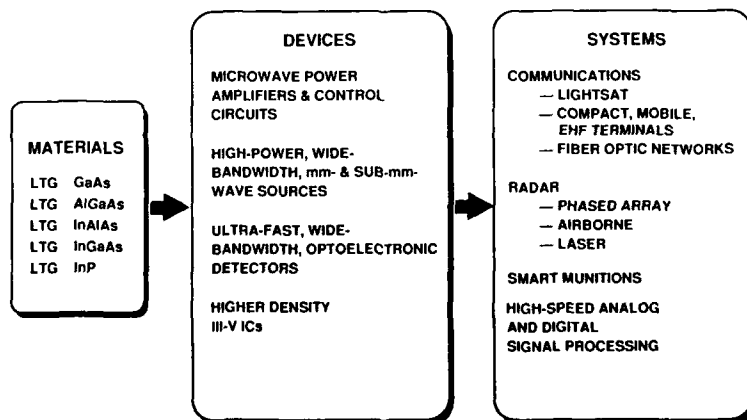


Figure 7 Illustration of the device and potential systems applications of LTG III-V materials.

GaAs photoconductive detectors can be used as ultrafast, wide-bandwidth, optoelectronic detectors for a variety of applications. Clearly the LTG GaAs buffer will continue to be used to achieve higher density ICs for microwave, optoelectronic, digital, and analog applications.

Possible systems applications of these devices include communications (e.g., satellites and fiber-optic-based systems), radar, smart munitions, and signal processing applications. The ability to monolithically integrate high-performance electronic and optoelectronic devices on the same substrate using the same LTG III-V material is a significant advantage for systems applications in which size, cost, reliability, and performance are factors.

CONCLUSIONS

The device applications of LTG GaAs have been reviewed. As a buffer layer in FETs, LTG GaAs has been shown to eliminate sidegating in GaAs ICs and has been shown to reduce short-channel effects in submicrometer-gatelength MESFETs. As a gate-insulating and surface-passivation layer in a MISFET configuration, LTG GaAs has led to record large breakdown voltages and high current density, which have resulted in record output power density (1.57 W/mm) from a GaAs-based FET. In photoconductive applications, LTG GaAs switches have achieved record switching speeds (0.5 ps) and peak voltages (1 kV) in picosecond electrical pulses, and LTG GaAs detectors have demonstrated high responsivity (0.1 A/W) with extremely wide bandwidth (375 GHz).

Since the first publications on LTG GaAs [1],[2], the properties and devices applications of LTG III-V materials have been the subject of increasingly active research. Including the papers included in this digest, there have been over 130 publications on LTG III-V technology in archival journals and texts in the last three years. Because of the novel properties of the materials, the profound performance advantages of devices based on these materials, and the manifold systems applications, LTG III-V materials should continue to be a fertile and growing area of research in the future.

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PART I

Electrical and Optical Properties
of LT GaAs

THE ELECTRICAL AND OPTICAL PROPERTIES OF GaAs WITH As PRECIPITATES (GaAs:As)

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ABSTRACT

Since its initial report by the IBM/Purdue University group in 1990, GaAs with As precipitates (GaAs:As) has been shown by this group to exhibit unusual and useful electrical and optical properties. In this paper we review our progress in understanding the fundamental properties of this material. We have shown that both the electrical and optical properties of GaAs:As are explained by assuming that the GaAs is of good crystalline quality and that the As precipitates act as buried Schottky barriers. This model accounts for its semi-insulating stability against both n- and p-type doping, its high-speed photoconductive behavior, and its ability to detect 1.3 micron light when it forms the "I" layer of a PIN photodiode via the internal photoemission process. Using modulation spectroscopy we clarify the fundamental differences between GaAs:As and unannealed GaAs grown at 200°C. We also show that GaAs:As used as a 1.3 micron detector in the metal-semiconductor-metal device structure format, has a photoconductive bandwidth in excess of 50 GHz.

INTRODUCTION

GaAs grown at 200-250°C and subsequently annealed at 600°C has proven valuable in both electronic and optoelectronic applications, but the source of its extremely high resistivity has been the subject of some debate.¹⁻⁴ A variety of characterization techniques were applied to both the as-grown and annealed layers, with several interesting results. As-grown material (LT-GaAs) was found to be highly strained, containing roughly 1-2% excess As and as high as $10^{20}/\text{cm}^3$ As-antisite defects (by electron paramagnetic resonance (EPR)),^{5,6} with essentially no photoluminescence response.⁷ The balance of the excess As is most likely distributed as interstitials, contributing to the strain. While the excess As

remained after anneal, the strain and point defects were eliminated (to resolution limits),⁶ and a fast photoluminescence response could now be observed.⁷

The change in material properties upon annealing was not understood until it was found that a substantial fraction of the excess As in the material actually precipitated out into macroscopic As clusters.^{6,8,9} A 600° C anneal was found to result in irregular precipitates with roughly 6 nm diameter and a volume density of $10^{17}/\text{cm}^3$, which, within experimental error, accounts for all the excess As.^{6,9} This corroborated the observations by EPR that defect densities were reduced from above 10^{19} to below the resolution limit of about $10^{18}/\text{cm}^3$. In addition, the photoresponse is consistent with the starting, heavily-defected LT-GaAs being converted into a high-quality, optically active GaAs matrix with embedded As precipitates (GaAs:As) which act as sparse recombination centers for photo-generated carriers. This was used to advantage in the fabrication of Terahertz-speed transceivers using GaAs:As as the photo-active material, which demonstrated turn-on speeds indistinguishable from that of bulk GaAs.¹⁰

With the observation of As precipitates in annealed LT-GaAs, Warren, et al. proposed a simple model for its electronic properties¹ which assumed that the observed As precipitates were metallic, and that the Schottky barrier height of As to GaAs held. In this model, As precipitates would be surrounded by depletion spheres in heavily doped material or completely deplete more lightly-doped GaAs, regardless of doping type. The principal alternative model is defect-mediated pinning by a deep donor as observed in un-annealed LT-GaAs.²⁻⁴ In the following sections we review the electronic properties of GaAs:As in light of these two models, and present further measurements of the dependence of sample resistivity on precipitate distribution, and of band bending and Fermi level pinning position in heterostructures containing un-doped GaAs:As. These data are shown to fit the simple Schottky model and are inconsistent with a defect-mediated Fermi level in this system.

THE COMPENSATION OF N AND P- DOPANTS BY As PRECIPITATES

The first prediction that falls out of the precipitate Schottky model is that there should be a clear relationship between doping, precipitate densities, and conductivity. When the doping density is high enough or the precipitate density low enough, individual precipitates will be surrounded by isolated depletion spheres which leave the material only partly compensated and therefore conducting. In the converse, the depletion regions overlap so that there are no free carriers and the material is semi-insulating. It has been observed that rapid thermal annealing (RTA) of a doped but previously non-conducting sample could be made conductive, or "activated".¹¹ Within our model, this could be explained if the excess As were being redistributed through precipitate "coarsening" which is driven by the tendency of the system to reduce its precipitate/matrix interfacial area.¹² To study this, n- and p-type wafers of several doping densities were grown using our standard LT-GaAs plus 600° C cap technique. Samples were then exposed to various RTA cycles and examined using cross-section trans-

	600	700	800	900
Diameter (nm)	5.5	7	15	20
Spacing (nm)	18	22.5	47.5	67.5
N_D ($\times 10^{15} \text{ cm}^{-3}$)	170	87	9.3	3.2
Volume fraction	0.015	0.016	0.016	0.014
n_{1E18} ($\times 10^{17} \text{ cm}^{-3}$)	—	0.003	4	5
μ_{1E18} ($\text{cm}^2/\text{V}\cdot\text{s}$)	—	420	1520	1950
n_{5E18} ($\times 10^{17} \text{ cm}^{-3}$)	—	1.2	7.5	11
μ_{5E18} ($\text{cm}^2/\text{V}\cdot\text{s}$)	—	680	1180	1320

Table 1. TEM and Hall data for as-grown and annealed (600° C), and RTA'd samples (700, 800 and 900° C). Top group is mean precipitate size and distribution data, while lower two groups are electron density and mobility for bulk doping levels of 1 and $5 \times 10^{18} / \text{cm}^3$.

mission electron microscopy (TEM) and Hall conductivity measurement of carrier densities and mobilities. Table 1 shows results from such measurements using n-type samples with nominal doping levels of 1×10^{18} and $5 \times 10^{18} / \text{cm}^3$ and exposed to a 30 second RTA cycle at 700, 800 or 900° C. Statistical means for precipitate diameter and volume density were extracted from the TEM measurements and confirm that the RTA is indeed causing a coarsening of the As distribution in favor of sparse, large precipitates.

The RTA "activation" of these doped samples is completely consistent with the observed precipitate coarsening, resulting in isolated "depletion spheres" which are decreasingly effective in compensating the doped GaAs. A simple calculation of Laplace's equation for an isolated precipitate can be used to estimate the amount of charge on it and therefore the amount of doping a precipitate could compensate. For example, a barrier height of 0.7 eV would result in about 18 excess electrons charge (on a 6 nm precipitate), so that $10^{17} / \text{cm}^3$ precipitates could compensate up to $2.3 \times 10^{18} / \text{cm}^3$ doping. Assuming uniform doping, this model gives a precipitate-size/conduction threshold of 5 nm for $5 \times 10^{18} / \text{cm}^3$ material, and 12 nm for 1×10^{18} , in agreement with the measured data in Table 1. The heavily doped samples do not fully activate, as could be expected if the doping concentration in the GaAs were correlated with the As precipitate location. This is consistent with measurements of impurity redistribution in heavily Si-doped, Arsenic-rich LT-grown GaAs during high temperature anneals.¹³

MODULATION SPECTROSCOPY OF LT-GaAs AND GaAs:As

In order to probe the electric fields in and adjacent to LT-grown layers, special heterostructure stacks were grown for electromodulation (EM) measurements. Here, n^+ (N) and p^+ (P) buffer layers (doped at $5 \times 10^{18}/\text{cm}^3$) were grown on like substrates, followed by a 50 nm undoped (U) GaAs i-layer at 600°C . At this point the temperature was dropped to 250°C and 150 nm of LT-GaAs was deposited for samples referred to as LTUN and LTUP, respectively. In other samples, this recipe was followed by an in situ ramp back up to 600°C , followed by a 20 nm cap of un-doped GaAs and 1 hour anneal at 600°C in an As_2 flux. These samples are referred to as ALTUN and ALTUP layers. Electric fields in these samples were then measured from the Franz-Keldysh oscillations (FKOs) observed using both photoreflectance (PR)¹⁴ and contactless electroreflectance (CER).¹⁵ These two techniques gave identical fields; in addition, CER gave the field sign from the phase of the reflected signal. In the LTUN structure, the measured field was $1.1 \times 10^5\text{ V/cm}$ which corresponds to the built-in field at the i-layer/ n^+ interface. This value places an upper limit of about 0.5 eV for the Fermi level distance from the conduction band edge at the LT/i-layer interface. In the LTUP sample, the measured field was $1.8 \times 10^5\text{ V/cm}$ which corresponds to a Fermi level position in the LT material of around 0.4-0.5 eV below the conduction band. These two measurements are exactly what one would expect from a single deep donor level 0.4 eV below the conduction band which corresponds to the EPR³ and infrared absorption¹⁶ measured As-antisite defect. Fig. 1 shows our modelling results for the LTUN case with such a defect, illustrating the lack of firm pinning for this system.

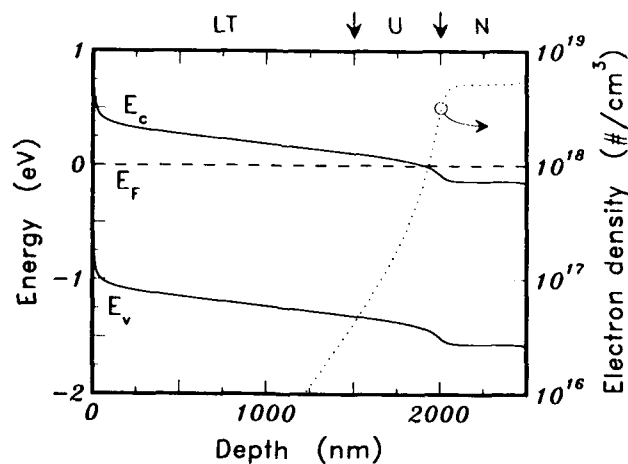


Figure 1. Band bending diagram for LTUN (un-annealed) structure. A deep donor is included in the LT material with energy 0.4 eV below the conduction band edge. Arrows indicate the interface between the LT, U and N layers.

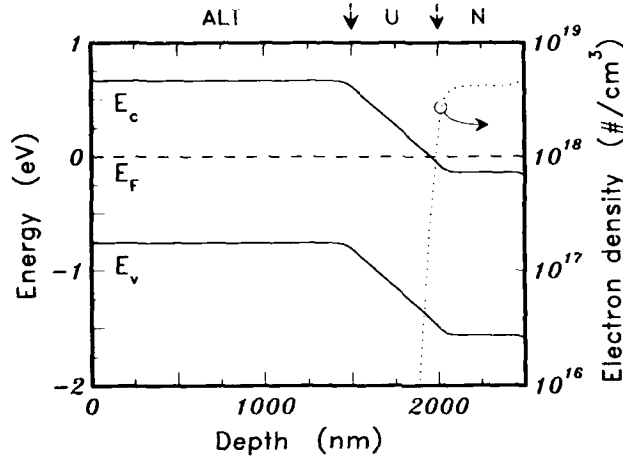


Figure 2. Band bending diagram for ALTUN (annealed) structure. The Fermi level in the ALT material is pinned at 0.67 eV below the conduction band edge (E_c) and includes a Debye tail of 9 nm at the ALT/U interface. Arrows indicate the interface between the ALT, U and N layers.

Data from the ALTUN and ALTUP samples, however, indicate a completely different system. The measured field in both samples was 1.25×10^5 V/cm, indicate a single mid-gap GaAs:As Fermi level position for both samples. Allowing for doping degeneracy and Debye tailing in the doped substrates, and an 8 nm Debye tail in the GaAs:As layer, our calculations yield equal fields of 1.3×10^5 V/cm with a pinning position of 0.67 eV below the conduction band edge. Modelling of the band bending for the ALTUN case is shown in Fig. 2, showing the extreme contrast between this case and the LTUN (un-annealed) one. The extrapolated pinning position is in excellent agreement with our measured Fowler-Nordheim photoresponse threshold of 0.7 eV,¹⁷ and is what one would expect from the barrier height of As to GaAs. In addition, it is clear that such pinning could not be produced by a single donor or acceptor defect.

The defect mediated compensation model is hard-pressed to explain the available data. First, both donor and acceptor levels at the same energy and with densities greater than mid $10^{18}/\text{cm}^3$ would be required to explain the ALT material's observed doping compensation. Second, these levels would have to have been created during the 600° C anneal, as they are not evident in the LT material. Third, in contrast to the EL2 level in LT-GaAs, these defects must be invisible to EPR and yield no discrete DLTS signal.¹¹ Fourth, they can have only negligible effect on carrier mobilities as found in THz optoelectronic transceivers.

Fifth, while being created by the 600°C anneal, they must be gradually removed by higher temperature RTA's in order to produce the observed doping "activation". And finally, these defects must be relatively transparent in the infrared, as early results clearly show the discrete level associated with EL2 being removed by annealing at 600° C leaving a uniform, clean GaAs background.^{6,11} To our knowledge, there are no defects in GaAs that fulfill these criteria. And while it is certainly probable that some low level of residual point defects in the GaAs matrix remain, their density is below the resolution limit of available detection methods and they cannot explain the observed optical and electronic properties.

1.3 MICRON GaAs:As MSM FAST PHOTODETECTOR

Fast photodetectors which operate at 1.3 or 1.55 μm wavelengths are of critical importance to integrated communications applications. Normal GaAs exhibits strong band-to-band absorption, but with a bandgap wavelength threshold of 820 nm. Strained InGaAs/GaAs superlattices on GaAs have recently been shown to have good responsivity and reasonably low leakage currents, but are difficult to grow, and must be pushed to high In mole fractions to operate in this wavelength regime¹⁸. Low temperature, MBE-grown GaAs (LT-GaAs) has been used successfully at short wavelengths as the active photoconductive component in photoconductors² and in a complete THz-speed transceiver system¹⁰. In these systems, either bulk defects or macroscopic As precipitates (formed by annealing the as-grown material) serve as recombination sites for the photo-generated electrons and holes.

Within GaAs having As precipitates (GaAs:As), absorption can also occur in the precipitates themselves, with photocarriers generated via emission over the 0.7 eV As/GaAs Schottky barrier. This has been used to produce PIN-configuration photodetectors with 2-2.5% internal quantum efficiency, having packaging and capacitance limited modulation speeds of 2 GHz¹⁹. In the following sections we report the fabrication of MSM photodetectors which reduce the extrinsic limitations, having modulation response bandwidths in excess of 50 GHz over a bias range of 2-35 V.

PHOTODETECTOR FABRICATION

Layer growth for these devices is extremely simple, consisting entirely of undoped GaAs and requiring a temperature change between a typical growth temperature of 600°C and 225°C. On a semi-insulating GaAs wafer a 2000 Å GaAs buffer layer was grown at 600°C, followed by 1 μm thick undoped GaAs layer grown at 225°C, and a 200 Å cap layer of 600°C GaAs. The transition between the different-temperature growth regions was achieved by continuing growth while the changed temperature equilibrated, resulting in "temperature-grade" regions of 2500 and 500 Å thick, below and above the LT-GaAs layer, respectively. The low temperature GaAs is exposed to 600°C during both the

growth of the top GaAs layer and a subsequent 60 minute anneal in an As_2 beam after growth has been completed. This process has been demonstrated⁸ to produce a high quality GaAs matrix containing As precipitates of roughly 70 Å diameter with a density of 10^{17} cm^{-3} . The device fabrication was performed using standard photo-lithographic techniques. The MSM-PD was buried within a ground-signal-ground coplanar stripline, with the Ti/Pt/Au MSM-PD fingers and stripelines defined in one mask step. The detector area was $75 \times 75 \mu\text{m}^2$, with finger spacings of $3 \mu\text{m}$.

The optical excitation pulses used in this experiment were generated from a 100 MHz repetition rate $1.3 \mu\text{m}$ Nd:YLF laser, focused into a dispersion shifted single mode fibre, which spectrally broadened and chirped the pulse. These pulses were then compressed using a double pass grating compressor²⁰. Typical pulse widths ranged from 700 to 900 fs. The electrical pulse generated by the detector was coupled into a calibrated 40 GHz Tektronix sampling head by a in-house high speed time domain probe²¹. The system rise time, including the probe and sampling head was approximately 13 ps.

MEASURED DEVICE PERFORMANCE

DC current-voltage measurements of a typical GaAs:As MSM-PD are shown in Fig. 3, for both below ($1.3 \mu\text{m}$) and above (820 nm) bandgap wavelengths. At low fields, both below and above bandgap photocurrent (and dark current) curves were proportional to bias, suggesting a photoconductive behavior, whereas above 10 V the $1.3 \mu\text{m}$ photocurrent showed a square law dependence.

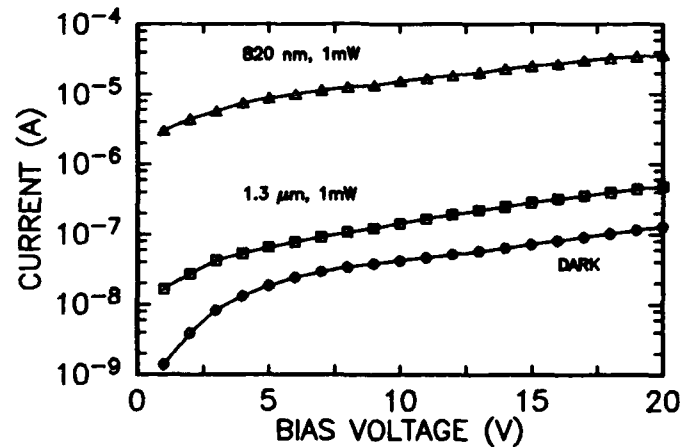


Figure 3. DC MSM dark current and photocurrent (1.3 and 0.82 micron wavelengths) as a function of bias voltage. Incident optical power for both photocurrent cases was 1 mW. Calculated responsivity at 20 V bias is 30 and 0.3 mA/W at 0.82 and 1.3 microns, respectively.

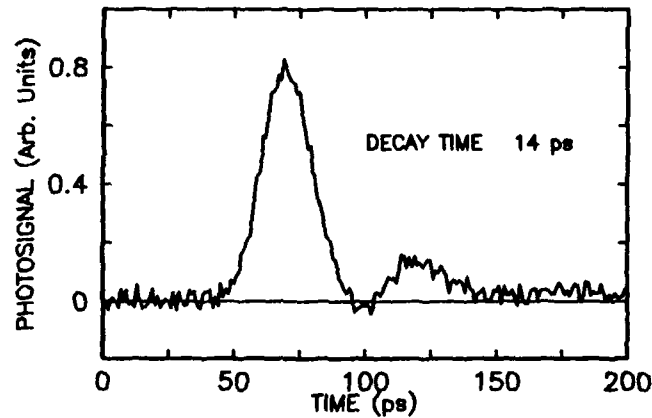


Figure 4. Impulse response of a GaAs:As MSM-PD with 3 micron finger spacing to an incident 1.3 micron, 1 ps excitation pulse. Rise and fall times were 14 ps, whereas the system limit is 13 ps.

This leakage current is comparable to that seen in conventional un-implanted GaAs MSM-PDs, where an excess current commonly known as low frequency gain²² (LFG) results from photocharging of trap states near the metal electrodes. This excess current results in a DC optical power dependence on the (dark current corrected) responsivity, in contrast to PIN photodiode results¹⁹. Measured MSM photocurrents are lower than unity-gain would imply as expected (due to reduced carrier lifetimes), with typical values at 20V bias of 30 and 0.3 μA at 820nm and 1.3 μm respectively, while dark current was about 0.1 μA . Correcting for LFG and subtracting out the dark current, we find the DC responsivity at 1.3 μm wavelengths to be 0.27 mA/W at 35V.

Figure 4 shows a typical impulse response of an GaAs:As MSM-PD to 1.3 μm light at a bias of 30 V. The measured pulse response is at our system limit with 10-90% rise and fall times of around 14 ps, independent of bias (from 2 - 35V). Integration of the pulse produced an estimated responsivity of 0.25 mA/W, in close agreement with the (corrected) DC value. In contrast with the DC results, we found no change in responsivity for the pulse data over the range of illumination intensities used (0.5 - 10 MW/cm²). By deconvolving the response of the probe and the scope from the temporal measurement (rise time of 13 ps), we obtain a detector bandwidth well beyond 50 GHz.

We find that the peak amplitude and the pulse area exhibit a linear dependence on bias voltage (Fig. 5). This is characteristic of photoconductive behavior rather than normal behavior observed in GaAs MSM-PDs, for which the photosignal saturates near unity gain at low biases. Also of interest, we note that if the detector is illuminated with about 100 μW of CW 633 nm light the peak response of the detector to the 1.3 μm pulse was increased by approximately 20%, without degradation of the temporal response.

Responsivity in such a system will depend on carrier lifetime, and somewhat on any screening of the electric field caused by charging of the As wells near the electrodes. For 820 nm wavelengths, the free carrier lifetime is approximately 2 ps¹⁰, and assuming a uniform field we would predict photoconductive gain of about 0.06 (upper limit). Our measurements yield a value of 0.035 - 0.1 (at 20V bias), suggesting that sufficient field for electron-hole separation does indeed extend throughout the gap. From examination of the voltage required for unity gain in "normal" GaAs PIN-PDs we estimate that the minimum field must be of the order of 2-4 kV/cm.

For 1.3 μm wavelengths, however, we observe photoconductive gain in the region of 0.01 - 0.016 (including correction for measured 3-5% absorption at this wavelength). We postulate that this reduction from that observed for above bandgap light is due to the field dependence on the escape probability for absorbing electrons. At 820 nm an electron-hole pair must be split, whereas at 1.3 μm you only obtain a contribution to the current if the absorbing electron can escape from its (immediately charged) precipitate and is likely to have a monotonic field dependence rather than exhibit a threshold. The expected charging of precipitates near the edge of the gap will partially screen the electric field, reducing the photocurrent contribution over much of the active area. Near the cathode on the other hand, electron emission from a charged precipitate could likely leave behind a neutral site which would be comparable to the general case for above bandgap illumination.

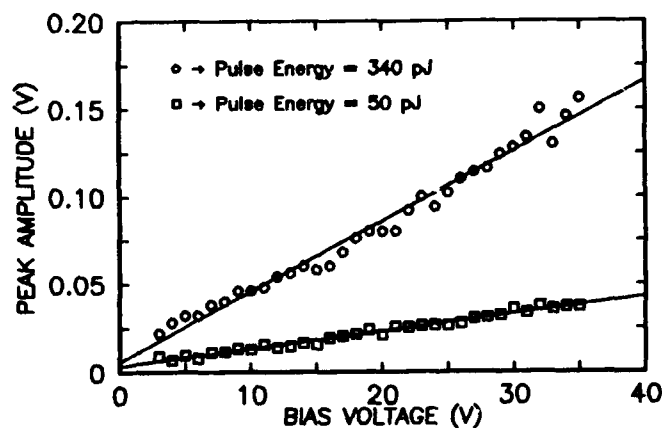


Figure 5. Peak amplitude of a GaAs:As MSM-PD response pulse, as a function of applied bias. The linear dependence is indicative of photoconductive behavior.

The frequency response of the detector will be strongly affected by where the photocarriers are excited. Carriers excited in the central, low-field region that escape from an As well, will move along the field line until they come under the influence of another charged well. This would suggest a minimum lifetime of ~ 200 fs, governed by the average spacing between wells (200 Å). Of course, carriers produced in the high field region will have longer transit times as their carrier path length is now limited by the probability of trapping in a neutral state (i.e. ~ 2 ps). If these absorption mechanisms are indeed the dominant factors, one would then expect the intrinsic bandwidth of the GaAs:As MSM-PD to be in the region of 0.5 - 5 THz, depending on which spatial region dominates the photocurrent production.

SUMMARY

In summary, we have presented new measurements of carrier compensation and band bending in GaAs:As, and shown that this data is consistent with our model of Schottky pinning at As precipitates formed during a 600° C anneal. Examination of these and prior data show that the electronic properties of this system are clearly inconsistent with a defect controlled model. While it is possible that earlier reports were misled through the examination of incompletely annealed samples, our results indicate that the electronic properties of LT-GaAs annealed at 600° C or above is completely controlled by the Schottky barriers between the resulting As precipitates and the surrounding GaAs.

Also, we have demonstrated a 1.3 μ m GaAs:As MSM-PD, with a bandwidth in excess of 50 GHz. Simple modelling suggests that the intrinsic bandwidth could be 10 to 100 times higher. The advantages of GaAs:As include simplicity of growth and compatibility with standard GaAs processing, and low leakage currents. Its single-carrier absorption suggests a potential speed greater than that for standard two-carrier photodetectors, and its absorption threshold of 0.7 eV suggests applications in characterizing high speed photodetectors operating at communication wavelengths (1.3 and 1.55 μ m).

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INCORPORATION OF SILICON IN LOW TEMPERATURE MOLECULAR BEAM EPITAXIAL GaAs

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ABSTRACT

The localized vibrational mode (LVM) of silicon donor (Si_{Ga}) in molecular beam epitaxial GaAs layers grown at various temperatures is studied using the infrared absorption technique. It is found that the total integrated absorption of this LVM is decreased as the growth temperature decreases. This finding suggests a nonsubstitutional incorporation of Si in GaAs layers grown at ~ 200 °C. On the other hand, an almost complete substitutional incorporation is obtained in GaAs layers grown at temperatures higher than 350 °C. Thermal annealing does not cause any recovery of the Si_{Ga} LVMs in present GaAs layers grown at ~ 200 °C.

INTRODUCTION AND EXPERIMENTAL TECHNIQUE

It has been shown recently¹ that the arsenic-rich molecular beam-epitaxial (MBE) GaAs layers grown at low temperature contain a large density ($\sim 10^{19} \text{ cm}^{-3}$) of deep defects that are related to the arsenic antisite (As_{Ga}) defect.^{2,3} This material when used as buffer layers in field-effect transistor devices can substantially reduce backgating and sidegating.⁴ For device applications and kinetic limitations⁵ of low temperature MBE GaAs, it is desired to dope this material with n- or p-type dopants. One method of studying the incorporation of dopants in this class of materials is to measure their localized vibrational mode frequencies (LVMs). The optical absorption technique has the advantage of evaluating the LVMs of isolated shallow impurities in GaAs regardless of their charge states.^{6,7} In this letter, we report on the optical absorption measurements of the Si_{Ga} LVMs in MBE GaAs layers grown at temperatures ranging between 200 and 580 °C. It is observed that the total integrated absorption of these LVMs is reduced as the growth temperature decreases suggesting a nonsubstitutional incorporation in layers grown at low temperatures. The effect of the thermal annealing on the Si_{Ga} LVM in layers grown at 200 °C will be presented.

The MBE layers were grown in Varian systems under normal, As-stabilized conditions, at a growth rate of $0.8 \mu\text{m/h}$. The beam equivalent As-to-Ga pressure ratio was about 20. The substrate was semi-insulating GaAs grown by the liquid-encapsulated Czochralski technique. The substrate temperature (T) was varied between 200 and 580 °C. The thickness was $20 \mu\text{m}$ for layers doped with Si. Infrared absorption measurements were made at 77 K with a BOMEM spectrometer. Silicon doped GaAs layers grown at $T \geq 350$ °C were electron irradiated at room temperature by

using a 2.1 MeV electron beam from a van de Graaff accelerator in order to reduce the free carrier absorption. A conventional Hall effect technique is used to measure the free carrier concentration and conductivity.

RESULTS AND DISCUSSIONS

The optical absorption of the isolated Si_{Ga} LVM recorded at 77 K is shown in Fig. 1 for five samples grown at different temperatures but doped with the same silicon density ($[\text{Si}] \sim 1 \times 10^{18} \text{ cm}^{-3}$). It is clear from this figure that the intensity of the Si_{Ga} LVM is decreased substantially in samples grown at $T \leq 250^\circ\text{C}$. Due to the free carriers absorption in samples grown at $T \geq 350^\circ\text{C}$, the Si_{Ga} LVM is observed only after irradiating these samples with a 2.1 MeV electron beam (dose $\sim 1 \times 10^{17} \text{ cm}^{-2}$). The peak position energy of the Si_{Ga} LVMs is about 383.5 cm^{-1} for all samples (within experimental error) except the sample grown at 200°C which shows an apparent shift toward a higher energy. This shift may be due to the stress (strain) present in the MBE layer.⁸

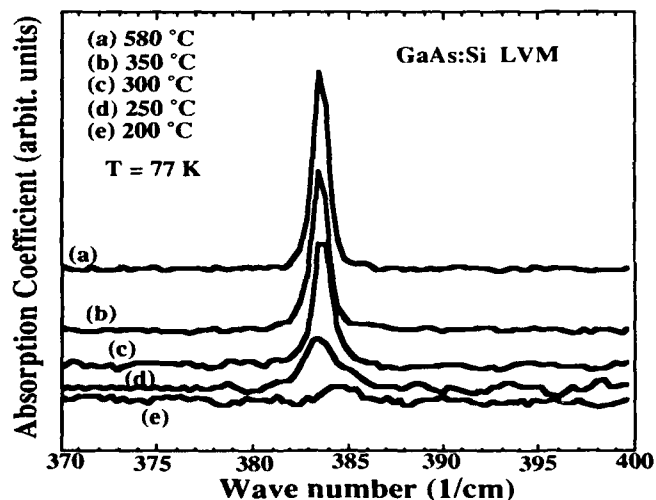


Fig. 1. The localized vibrational mode of Si_{Ga} in MBE GaAs grown at different temperatures. Spectra (a) and (b) were obtained after irradiating the samples with a 2.1 MeV electron beam. The spectra were recorded at 77 K.

The total integrated absorption of the Si_{Ga} LVM is plotted in Fig. 2 as a function of the growth temperature. The reduction of the LVM intensity as the growth temperature is decreased indicates a reduction of the substitutional incorporation of silicon in MBE GaAs. A trend similar to that of Fig. 2 was observed⁹ in the total carrier concentrations in GaAs:Si and

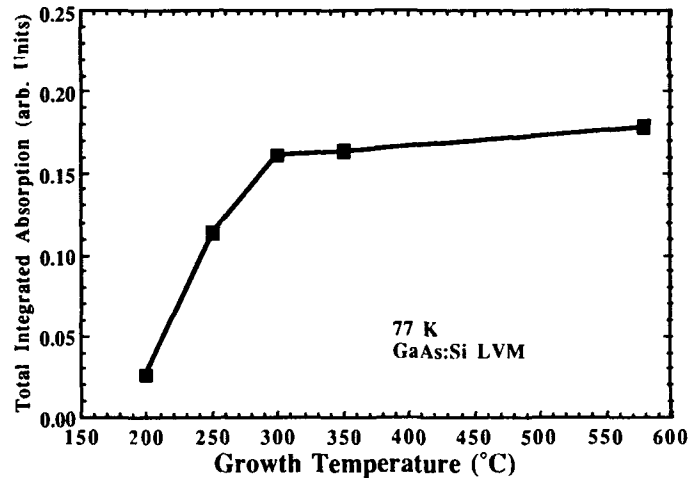


Fig. 2. The total integrated absorption of the localized vibrational modes of Si_{Ga} in MBE GaAs as a function of growth temperature.

AlGaAs:Si grown at temperatures ranging between 350 and 620 °C. The important conclusion here is that the substitutional incorporation rate of Si_{Ga} in MBE GaAs samples grown at $T < 250$ °C is very small as compared to that of samples grown at $T > 300$ °C.

The thermal annealing effect on the Si_{Ga} LVM in GaAs grown at 200 °C is shown in Fig. 3. Spectrum (a) in this figure is the same as spectrum (e) in Fig. 1. Figure 3 (b) is recorded after furnace annealing the same sample [spectrum (a)] at 600 °C for 20 min. The total integrated absorption of the LVM in spectrum (b) is almost doubled after the furnace anneal suggesting that a fraction of the silicon atoms are incorporated at the regular Ga-site. However, rapid thermal annealing at 850 °C for 15 s seems to substantially reduce the silicon substitutional incorporation as shown in Fig. 3 (c).

The Si_{Ga} LVM results described here have a relevance with regard to compensation in low temperature MBE GaAs. Basically, two compensation models have been proposed to explain the high resistivity in annealed low temperature MBE GaAs: (1) a "point-defect" model in which a deep donor N_{DD} (As_{Ga} related defect) compensates a shallow acceptor N_{SA} , leaving the Fermi level near mid-gap; and (2) an "As-precipitate" model in which large (~ 60 Å), dense ($\sim 10^{17} \text{ cm}^{-3}$) precipitates of metallic As produce overlapping Schottky depletion regions as a result of attracting the free carriers to the metal.¹⁰ If the depletion regions strongly overlap, the whole volume of the sample is essentially held at the Schottky potential, which is also near mid-gap. Let us first suppose that each of the shallow donor (N_{SD}) Si_{Ga} in the present samples contributes one conduction electron to the sample. Then low resistivity would be expected

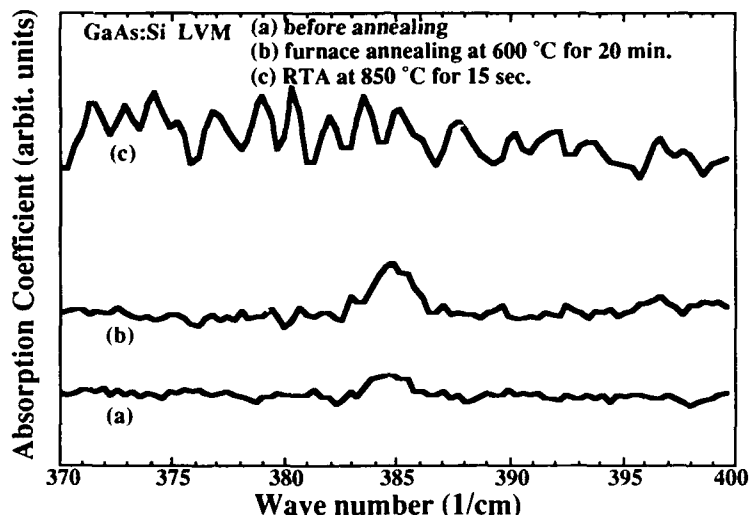


Fig. 3. The effect of thermal annealing on the Si_{Ga} localized vibrational mode in a GaAs sample grown at 200 °C. Spectrum (a) is obtained before thermal annealing, spectrum (b) is recorded after furnace annealing the sample at 600 °C for 20 min, and spectrum (c) is recorded after rapid thermal annealing (RTA) the sample at 850 °C for 15 sec. All spectra were recorded at 77 K.

unless (1) the As-precipitates were active, or (2) $N_{\text{SA}} > N_{\text{SD}}$ and N_{SA} were not too far below mid-gap. Indeed, N_{SA} can be quite large^{2,3} ($>10^{18}\text{cm}^{-3}$) from electron paramagnetic (EPR) results in unannealed, 200 °C -grown MBE GaAs, but it is much lower in annealed materials, as determined by the lack of an As_{Ga}^+ related

EPR signal. Thus N_{SA} in annealed material cannot compensate 10^{19}cm^{-3} silicon atoms if each is electrically active (i.e. Si_{Ga}), and the As-precipitate model (or some totally different mechanism) must be invoked. However, the present Si_{Ga} LVM results show that Si is mostly not electrically active in either unannealed or annealed, 200 °C-grown MBE GaAs. Therefore, there is no need to invoke the As-precipitate model to explain the lack of conductivity in this material. It might be noted that 300 °C - grown MBE GaAs can be made particularly conductive ($\sim 10^{15}\text{cm}^{-3}$) by doping with Si. According to a recent tunneling electron microscope (TEM) analysis of precipitates in material grown at 300 °C and annealed at 600 °C, about $0.78 \times 10^{16}\text{cm}^{-3}$ precipitates of average diameter 76 Å would be expected.¹¹ A further analysis then suggests that about 20% of the sample volume would be depleted of free carriers.¹² However, an actual increase of the free carriers concentration is observed by Hall measurements. In any case, a more definitive study, combining Si doping, annealing at various temperatures, TEM analysis, and

Hall measurements will have to be carried out to determine if As-precipitate model has validity. The results of the present study simply state that this model is not needed to explain the high resistivity.

CONCLUSION

In conclusion, the optical absorption of the localized vibrational modes of Si_{Ga} in MBE GaAs are studied for the first time as a function of growth temperature. The total integrated absorption of these localized vibrational modes is found to decrease as the growth temperature decreases suggesting a nonsubstitutional incorporation in samples grown at temperature less than 300 °C. Post-growth thermal annealing of silicon doped samples grown at 200 °C does not seem to significantly increase the substitutional incorporation of Si_{Ga}. The present results regarding the Si_{Ga} LVM in 200 °C - grown MBE GaAs suggest that the As-precipitate model¹⁰ is not needed to explain the high resistivity in this type of material.

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TRANSPORT MODELING AND COMPENSATION MECHANISM FOR SEMI-INSULATING LT-GaAs AND InP: Cu

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ABSTRACT

The compensation mechanism and transport properties of annealed GaAs grown by molecular beam epitaxy at low substrate temperature (LT-GaAs) and Cu diffused InP are analyzed by using a deep donor band model and a precipitate model. It was found that the compensation in highly resistive LT GaAs can not be explained by the precipitate model alone, and therefore a high donor density had to be considered. In Cu diffused InP, the precipitate model gives a consistent explanation for the observed carrier compensation and mobility data. For both semi-insulating LT-GaAs and fully-compensated, lightly-doped InP:Cu, the neutral impurity scattering was found to be a major carrier scattering mechanism.

INTRODUCTION

Since Smith and Calawa [1] first reported the molecular beam epitaxy (MBE) growth of GaAs layer at low substrate temperature (LT-GaAs) and its successful application as a buffer layer in FET devices, there has been a great progress made in both application and understanding of material properties of LT-GaAs [2-6]. LT-GaAs is highly resistive after annealing at 600°C. It is known that, in LT-GaAs, there exists over 1 at% excess As. As_{Ga} antisite defects are on the order of $10^{19}/cm^3$ in as grown LT-GaAs[3], and As precipitates are on the order of $10^{17}/cm^3$ in 600°C annealed LT-GaAs[5]. The unusual high density defects play a key role in determining the LT-GaAs material properties. In regarding to the compensation mechanism, there are two models: deep donor band model proposed by Look et al.[6] and As precipitate model by Warren et al.[7]. In Look's model, a EL2 deep donor band is assumed as the major compensation centers, similar to the case of undoped semi-insulating bulk GaAs, except the density of EL2 level is much higher in LT-GaAs. It was reported that the high density of EL2 level in LT-GaAs annealed above 500°C was measured by the photoabsorption measurement[8]. However, this model failed to explain the semi-insulating behavior of annealed Si doped LT-GaAs. Based on the transmission electron microscopy (TEM) observation, Warren et al. suggested that overlapping of the depletion regions surrounding the As precipitates could explain the semi-insulating behavior of both undoped and doped LT-GaAs. Recently, Leon et al. [9] reported that Cu diffusion in InP could lead to the formation of semi-insulating InP. It was suggested that Cu precipitate may be responsible for the semi-insulating properties of InP:Cu based on the TEM observation. Thus, it is of great interest to analyze the compensation and transport properties of both LT GaAs and InP: Cu based on the two models.

COMPENSATION AND TRANSPORT PROPERTIES OF LT-GaAs

The 5 μm thick undoped LT-GaAs layer grown at 200°C was used in this study. There is

2.5 at% excess As in this material. The detailed structural and electrical properties were reported in Ref. 4. Fig. 1 and 2 show the carrier concentration and mobility data as a function of measurement temperature for a 600°C RTA annealed sample. The reduction of mobility at and below room temperature is due to the hopping conduction [4]. From the charge neutrality condition, the following expression for electron density in conduction band can be obtained.

$$n_c = 1.85 \times 10^5 \times \left(\frac{N_D}{N_A} - 1 \right) \times T^{1.5} \times \exp \left(-\frac{E_{DO}}{RT} \right) \quad (1)$$

where N_D is the donor concentration, N_A is net acceptor concentration, and E_{DO} is activation energy of the deep donor level. The mobility is calculated by using Matthiessen's rule. $\mu^{-1} = \mu_i^{-1} + \mu_n^{-1} + \mu_{po}^{-1}$ where μ_i is ionized impurity scattering limited mobility, μ_n is neutral impurity scattering limited mobility and μ_{po} is polar-optical-phonon scattering limited mobility. As shown in Fig. 1 and Fig. 2, the experimental data were fitted fairly well by the calculated curves, with the parameters chosen at $N_D = 2 \times 10^{18}/\text{cm}^3$, $N_A = 5 \times 10^{14}/\text{cm}^3$, $E_{DO} = 0.75$ eV. The electron mobility is limited by neutral impurity scattering. More detail discussion can be found in Ref. 4 and 6.

In the precipitate model, the depletion width R of the As-GaAs Schottky junction is determined by solving Poisson's equation [7].

$$2R^3 - 3R^2 \bullet r + r = \frac{6\epsilon r}{qN_D} \Psi \quad (2)$$

where Ψ is the barrier weight, N_D is doping density, and r is precipitate size. We assume that the average size of precipitate is 30 Å and precipitate density is on the order of $10^{17}/\text{cm}^3$. The Fermi level at the As-GaAs interface is assumed to be pinned at 0.8 eV below the conduction band. From the experimental data, the room temperature electron density in conduction band is

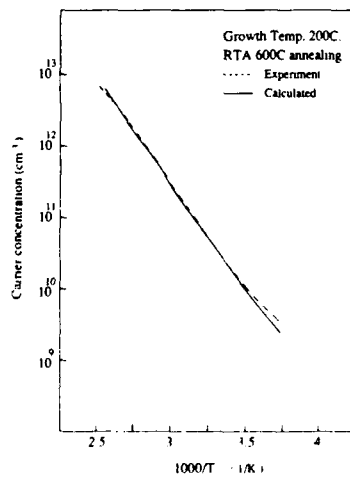


Fig.1 Temperature dependent carrier concentration of LT-GaAs.

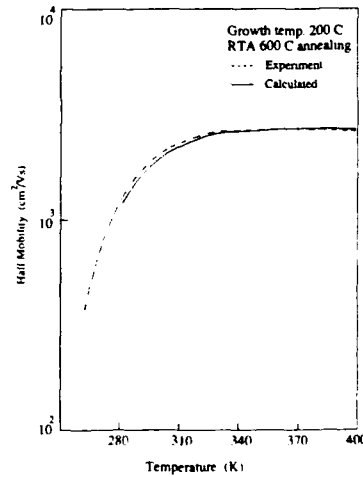


Fig.2 Temperature dependent Hall mobility of LT-GaAs.

$1.9 \times 10^{10}/\text{cm}^3$. So the Fermi level is at $E_c - 0.44 \text{ eV}$ at midway between neighboring As precipitates. From Eq. (2), if N_D is below $10^{16}/\text{cm}^3$ which is a typical shallow impurity concentration in undoped MBE GaAs layer, then the depletion region would be totally overlapped and Fermi level should lie at around 0.8 eV below the conduction band. Apparently, this is not the case for this LT-GaAs. In order that Fermi level is located at $E_c - 0.44 \text{ eV}$, a high density of donor impurity level larger than $1 \times 10^{18}/\text{cm}^3$ is required. The above discussion indicates that the deep donor band in this LT-GaAs may play an important role in determining the compensation level.

The electron movement in LT-GaAs with presence of As precipitates can be a complicated process. The space charge region may be assumed to be an impenetrable object to electrons. The scattering effect depends on the barrier height. A simple approximation was used to estimate the electron mobility limited by the impenetrable objects [10]

$$\mu = \frac{9.2036 \times 10^9}{(N_p \sigma) \cdot T^{1/2}} \quad (\text{cm}^2/\text{Vs}) \quad (3)$$

where N_p is density of impenetrable objects and σ is scattering cross section. From the Fermi level position, the As-GaAs junction barrier height is determined to be $\Psi = 0.36 \text{ eV}$. The minimum space charge region width ($R = 120 \text{ \AA}$) is calculated based on Eq. (2) if all deep donors are assumed to contribute to the formation of space charge region. The scattering cross section is taken to be πR^2 [11]. Then $N_p \sigma$ product is $5 \times 10^5 \text{ cm}^{-1}$ with $N_p = 1 \times 10^{17}/\text{cm}^2$. Between 300 K and 400 K , the mobility calculated from Eq. (3) is less than $1000 \text{ cm}^2/\text{Vs}$ which is smaller than measured mobility ($> 2000 \text{ cm}^2/\text{Vs}$). This shows that scattering by precipitate is not the dominant mechanism. Look also gave a similar conclusion in his recent paper [12]. It should, however, be noted that the presence of As precipitates in this LT-GaAs sample has not been verified yet.

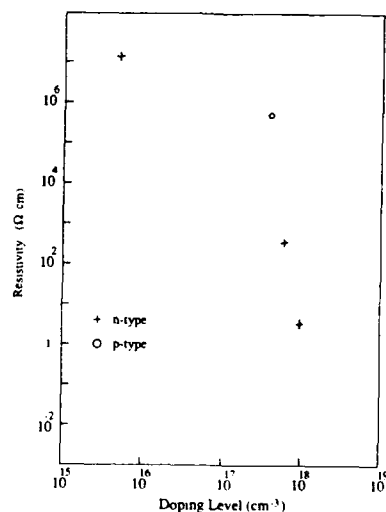


Fig.3 Resistivity of InP with different background doping level after 800°C Cu diffusion for 20 hours and 15s RTA annealing at 350°C

COMPENSATION AND TRANSPORT PROPERTIES OF InP:Cu

Cu diffusion in InP was performed by evaporating a thin Cu film onto InP wafer surfaces and then annealing it in an evacuated ampoule at 800°C for 24 to 36 hrs. All samples were processed under identical conditions. It was found that both n type and p type InP could be compensated and become highly resistive without changing the type. Auger electron spectroscopy (AES) measurement showed that Cu concentration is below the AES detection limit which is about 1 at%. Fig. 3 shows the room temperature resistivity data as a function of the back ground doping level in InP wafers after 350°C, 15s RTA annealing. It is seen that the resistivity decreases with the increasing background doping level, and the compensation is more effective in p-type InP. It is not clear at present time whether Cu impurity would form a deep donor level or acceptor level in InP. It is obvious that simultaneous compensation of n-type and p-type material can not be explained by the deep level model alone if Cu impurity would only form a donor or acceptor level. It is known that Cu is a double acceptor in GaAs. As a comparison, Cu diffusion was performed in n-type and p-type GaAs with identical procedure as that for InP:Cu. It was found that there is no carrier reduction in Cu diffused p-type GaAs. However, after Cu diffusion at 700°C, n-type GaAs with $5 \times 10^{16}/\text{cm}^3$ doping level converted into a conductive p-type GaAs and n-type GaAs with $1.5 \times 10^{18}/\text{cm}^3$ doping level became a highly resistive p-type GaAs. Cu diffusion at a higher temperature would convert all n-type GaAs into conductive p-type material. This indicates that compensation of electron in GaAs:Cu is due to the Cu acceptor levels[13].

A TEM study of Cu diffused InP has shown the formation of Cu precipitates [9]. Therefore the Cu precipitate compensation model appears to be a plausible model. Fig. 4 and Fig. 5 show the temperature dependent carrier concentration and mobility data for the Cu diffused n-type InP with the background doping level at $5 \times 10^{15}/\text{cm}^3$, $6 \times 10^{17}/\text{cm}^3$ and $1 \times 10^{18}/\text{cm}^3$. The reduction of mobility in partially compensated samples is most interesting. Before Cu diffusion, the room temperature mobility values were 4000 cm^2/Vs for the sample with $5 \times 10^{15}/\text{cm}^3$ doping level, 2560 cm^2/Vs for the sample with $6 \times 10^{17}/\text{cm}^3$ doping level and 1700 cm^2/Vs for the sample with $1 \times 10^{18}/\text{cm}^3$ doping level. If the reduction of mobility in the Cu diffused samples was due to the impurity or defect scattering only, it would be expected that all three samples show similar

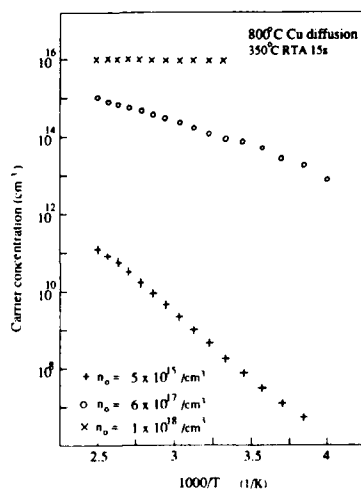


Fig. 4 Temp.-dependent carrier concent.

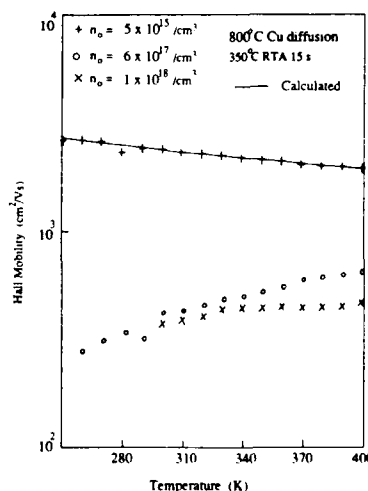


Fig. 5 Temp-dependent Hall mobility.

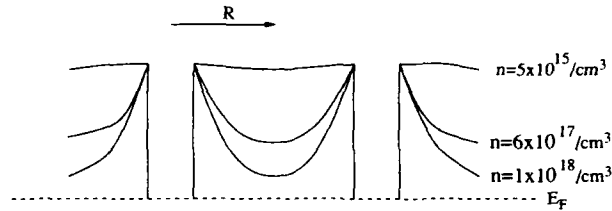


Fig.6 The overlapping of space charge region as a function of doping level

mobility data. But this is not the case. Qualitatively, the mobility data can be explained by the Cu precipitate model. For a given density and size of precipitates, depletion regions overlap less when the doping level is higher as shown in Fig. 6. Electrons will experience a high barrier height in the less compensated sample. Thus the scattering due to space charge region will be stronger. When the depletion regions are fully overlapped as shown in Fig. 6, scattering due to precipitates will be greatly reduced. As shown in Fig. 3, the undoped InP:Cu has the highest resistivity and mobility among the three samples. The Fermi level of this sample is at $E_c - 0.57$ eV. So it can be assumed that the depletion regions are fully overlapped in undoped InP:Cu. It was found that the temperature dependent mobility of this undoped ($n = 5 \times 10^{15}/\text{cm}^3$) InP:Cu could be fitted by neutral impurity scattering combined with the polar-optical phonon scattering. The combination of $T^{-1/2}$ dependent mobility and polar-optical-phonon scattering limited mobility could not fit the experimental data. This suggests that, for fully compensated sample, the effect of precipitates on the mobility is not significant.

Carrier concentration data offered another interesting observation. The Fermi level in each sample is estimated from room temperature carrier concentration as listed in Table I. The Fermi level is assumed to be pinned at $E_c - 0.55$ eV of the interface of Cu-InP Schottky junction. The Cu precipitate size is assumed to be less than 100Å. With these assumption, it is found that the space charge region R calculated based on Eq. (2) for two high doping samples are close to each other, with r varying from 40Å to 80Å. The R value is listed in table 1 for $r = 80$ Å. This suggests that compensation in these two high doping samples can be explained by precipitate model as well. However, there is question regarding a possible Fe contamination in Cu diffused InP. Fe is a compensating acceptor in InP with activation energy $E_t = 0.65$ eV which is close to the activation energy of carrier concentration ($E_a = 0.62$ eV) in the lowest background doping InP:Cu. If

Table I

Doping Level $n_0 (\text{cm}^{-3})$	Carrier Concent After Diffusion $n_d (\text{cm}^{-3})$	Fermi ^a Level $E_c - E_F (\text{eV})$	Space Charge ^b Region Size $R(\text{Å})$
1×10^{18}	5.6×10^{15}	0.121	246
6×10^{17}	5.03×10^{13}	0.243	251
5×10^{15}	1.43×10^8	0.568	

a. The Fermi level was calculated from carrier concentration for the diffused samples.

b. The space charge region size was calculated from Eq.(2).

this is the case, InP:Cu should show similar behavior to that of GaAs:Cu. It is believed that Fe contamination is not significant in InP:Cu material.

SUMMARY

For RTA annealed, highly resistive LT-GaAs, the deep donor level may play a significant role in the compensation mechanism. The transport properties are determined by the impurity scattering. In InP:Cu, Cu precipitates were considered as a responsible mechanism for the high resistivity. For partially compensated InP:Cu material, the electron mobility was affected by the precipitates. However, the electron mobility of fully compensated InP:Cu are controlled by the neutral impurity scattering.

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INSULATING AND BREAKDOWN CHARACTERISTICS OF LOW TEMPERATURE GaAs

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ABSTRACT

The electrical characteristics of an N(LT)N structure are studied through implementation of numerical simulation techniques for the case of donor traps 0.83 eV below the conduction band and acceptor traps 0.3 eV above the valence band. The results show characteristics sensitive to the relative densities of the traps. In particular, high acceptor trap / low donor trap concentrations generally result in low breakdown voltages, whereas high acceptor / high donor concentrations result in higher breakdown voltages.

INTRODUCTION

The purpose of this discussion is to briefly summarize recent calculations of the electrical characteristics of low temperature growth GaAs (LT GaAs). The device studied was a three micron N(LT)N structure with N regions characterized by shallow donors at $10^{17}/\text{cm}^3$; and an LT region characterized by a single level of acceptor traps of density P_a , located 0.3 eV above the valence band [1], and a single level of donor traps of density N_d located at 0.83 eV below the conduction band.

The results are placed in two categories: Highly resistive LT regions ($> 10^6$ ohm-cm) with (a) low current levels and sudden breakdown, and (b) higher current levels with gradual breakdown. Breakdown characteristics depend upon the magnitude and distribution of the field. For high acceptor / low donor trap concentrations the field is near zero in the LT region and approaches breakdown values at the anode (LT)N interface; for other combinations the field profile is complex. The study suggests that breakdown voltages will depend upon growth and processing temperatures of LT GaAs.

THE GOVERNING EQUATIONS

The equations include rate equations for electrons and holes, acceptor and donor traps:

$$(1) \quad \partial n / \partial t - \text{div}(j_n / e) = G + \{c_{nd}[n_d N_d^0 - n N_d^+] + c_{na}[n_a P_a^- - n P_a^0]\}$$

$$(2) \quad \partial p / \partial t + \text{div}(j_p / e) = G + \{c_{pa}[p_a P_a^0 - p P_a^-] + c_{pd}[p_d N_d^+ - p N_d^0]\}$$

$$(3) \quad \partial P_a^- / \partial t = -c_2 P_a^- + c_3 P_a^0$$

$$(4) \quad \partial N_d^+ / \partial t = -c_4 N_d^+ + c_1 N_d^0$$

Superscripts denote ionized and neutral acceptors and donors; particle currents are:

$$(5) \quad j_n = -e[nv_n - D_n \text{grad}n], \quad j_p = e[pv_p - D_p \text{grad}p]$$

and diffusivities are governed by the Einstein relation. Avalanche generation [2] is:

$$(6) \quad G = a_n[\exp(-(b_n/|F|)^m)]|j_n|/e + a_p[\exp(-(b_p/|F|)^m)]|j_p|/e$$

and the emissivity coefficients $e_1 \dots e_4$ are:

$$\begin{aligned}
 (7) \quad c_1 &= c_{nd}n_d + p c_{pd} & c_2 &= c_{na}n_a + p c_{pa} \\
 c_3 &= c_{pa}p_a + n c_{na} & c_4 &= c_{pd}p_d + n c_{nd}
 \end{aligned}$$

c_{nd} , c_{na} , etc., are capture coefficients [3]; n_d , p_d , etc., are obtained at equilibrium. The above equations are coupled through Poisson's equation, which in terms of energy is:

$$(8) \quad \nabla^2 E = -[e^2/\epsilon][(n-p) - (N_d^+ - P_a^-)]$$

The energy and potential are related, $E = -e\phi$; the field in equation (6) is $F = -\nabla\phi$.

THE RESULTS

All calculations were for the figure 1 shallow doping distribution, with the results dependent upon: (i) the Fermi level, (ii) the ratios P_a/N_d , and (iii) the trap density.

Low Bias Results: Resistivities and compensation estimates were obtained at low bias levels from the density distributions within the interior of the LT region. At a bias of 1.0 volts the results are similar to those at zero bias. As seen in table 1, the resistivities exceed 10^6 ohm-cm for donor traps at 10^{18} , and acceptor traps between 10^{17} and 10^{16} . The positions of the equilibrium Fermi level (above the valence band) for $N_d = 10^{18}$, and $N_a = (10^{18}, 10^{17}, 10^{16})$ are $E_f(\text{ev}) = (0.69, 0.63, 0.45)$, respectively. For $N_d = 10^{19}$, and $N_a = 10^{18}$, $E_f = 0.63\text{ev}$. The designation 'p' identifies the region as p-type, with the mobility dominated by holes. Table 2 displays the ionization of the traps at 1.0 v. The results indicate that within the insulating LT region $P_a^- \sim N_d^+$.

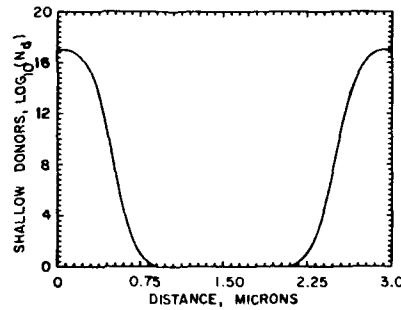


Figure 1. Shallow donor concentration of the $N(\text{LT})N$ structure.

$N_d(^+)/P_a(^-)$	10^{18}	10^{17}	10^{16}	10^{15}
10^{19}	2.72×10^8 (p)	••	••	••
10^{18}	3.21×10^8 (p)	2.68×10^8 (p)	9.24×10^8 (n,p)	4.75×10^7 (n)
10^{17}	5.49×10^1 (p)	3.18×10^3 (p)	2.45×10^8 (p)	••
10^{16}	7.16×10^0 (p)	••	••	••

Table 1. Resistivities (ohm-cm) of the LT region at 1.0 v.

$N_d(+)/P_a(-)$	10^{18}	10^{17}	10^{16}	10^{15}
10^{19}	$P_a^- \sim P_a$ $N_d^+ \sim 0.1N_d$	••	••	••
10^{18}	$P_a^- \sim P_a$ $N_d^+ \sim N_d$	$P_a^- \sim P_a$ $N_d^+ \sim 0.1N_d$	$P_a^- \sim P_a$ $N_d^+ \sim 0.01N_d$	$P_a^- \sim P_a$ $N_d^+ < P_a$
10^{17}	$P_a^- \sim 0.1P_a$ $N_d^+ \sim N_d$	$P_a^- \sim P_a$ $N_d^+ \sim N_d$	$P_a^- \sim P_a$ $N_d^+ \sim 0.1N_d$	••
10^{16}	$P_a^- > N_d$ $N_d^+ \sim N_d$	••	••	••

Table 2. Approximate compensation conditions in LT region at 1.0 v.

Finite and High Bias, $N_d \approx 0$: E_f is significantly below midgap. The results for: (i) P_a varying from $10^{14}/\text{cm}^3$ to $10^{16}/\text{cm}^3$, and (ii) $P_a > 10^{16}/\text{cm}^3$, are distinctly different. For P_a varying from $10^{14}/\text{cm}^3$ to $10^{16}/\text{cm}^3$, and at low voltage, charge neutrality within the LT region means $p \approx P_a^-$; and n is negligible. At elevated bias levels electrons are injected into the LT region and trapped by the acceptors. At sufficiently high bias, with the acceptor traps filled there is a significant increase in n , and a significant current increase. The electric field profile increases nearly linearly with distance. Further increases in bias result in avalanche multiplication. For larger P_a , higher bias is required to fill the acceptors, but the field profile within the structure is still linear. The relevant profiles for this calculation at a bias prior to breakdown are shown in figure 2, for $P_a = 10^{16}/\text{cm}^3$. For $P_a > 10^{16}/\text{cm}^3$, the kinetics is primarily that of holes within the valence band and the ionized deep acceptors, whose concentration is approximately two orders of magnitude below the total trap density. There is near charge neutrality within the LT region except at the downstream (LT)N interface where a high concentration of ionized acceptor traps forms, with a reduction of mobile holes. There is also a zone depleted of electrons within the heavily doped N region. One observes the formation of a pn junction region as a result of the trap dynamics, with the generation of a local high value of electric field. As a result *avalanching occurs at lower values of voltage, than for the lower P_a study.* The high P_a study is displayed in figure 3.

The situation for $N_d \neq 0$ is qualitatively different, although there are ostensible similarities. For example with $N_d = 10^{17}/\text{cm}^3$ and $P_a = 10^{18}/\text{cm}^3$ the field profile is qualitatively similar to figure 3. The difference is that the acceptor ionization is accompanied by ionized deep donors, as seen in figure 4. The breakdown characteristics are similar to the $N_d = 0$ study. The situation when $N_d = P_a = 10^{18}/\text{cm}^3$, displays characteristics that appear as a hybrid of the calculations of figures 2 and 3. At voltages up to and near 20 volts the field distribution is qualitatively similar to that of figure 3, although the peak field is approximately 60 kv/cm less. Further bias increases result in modest changes in the n and p profiles within the LT region, but an increasing share of the voltage drop across the LT region. Breakdown occurs at much higher voltage levels. *The current voltage characteristics for a select set of trap densities are displayed in figure 5. The trap density dependence of breakdown is shown in table 3.*

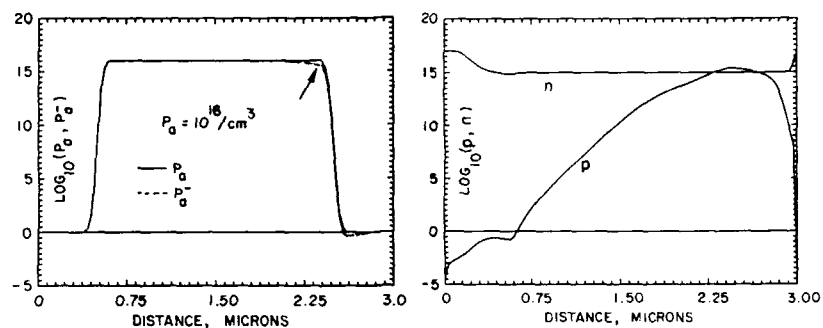


Figure 2. (a) Total and ionized trap distribution at a bias of 45 v. (2b). Distribution of electrons and holes.

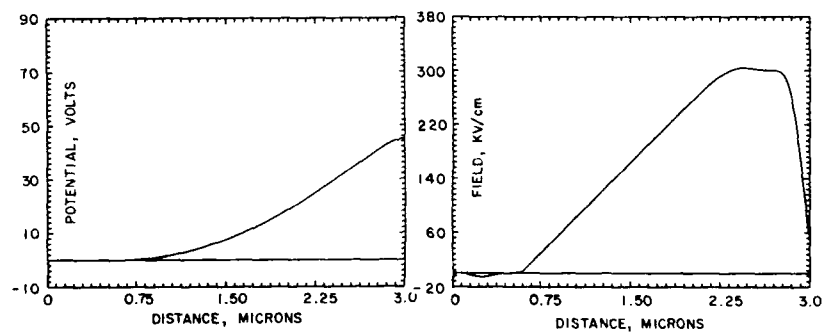


Figure 2c. Potential and electric field distribution at 45 v.

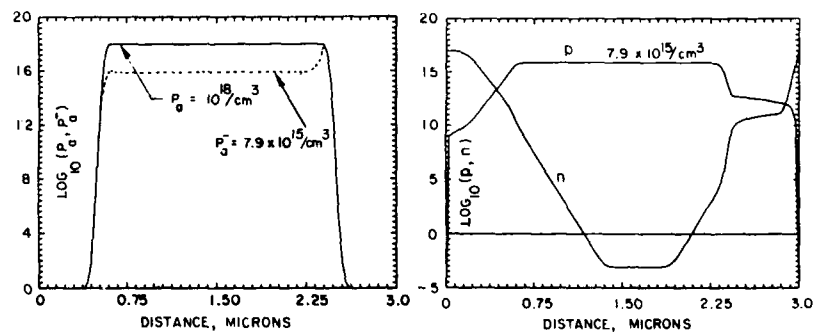


Figure 3. (a) Total and ionized trap distribution at 21v. (3b). Distribution of n and p .

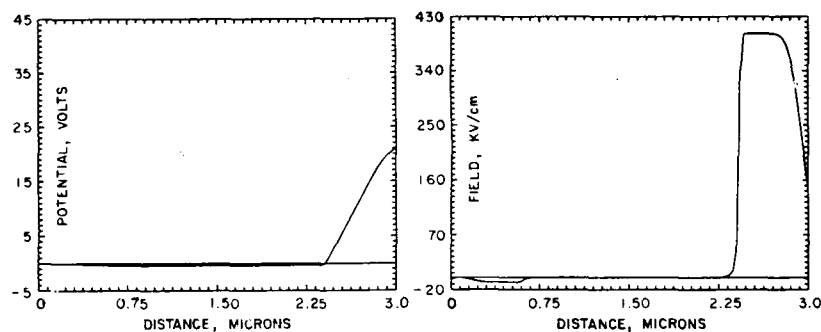


Figure 3c. Potential and electric field distribution at 21 v.

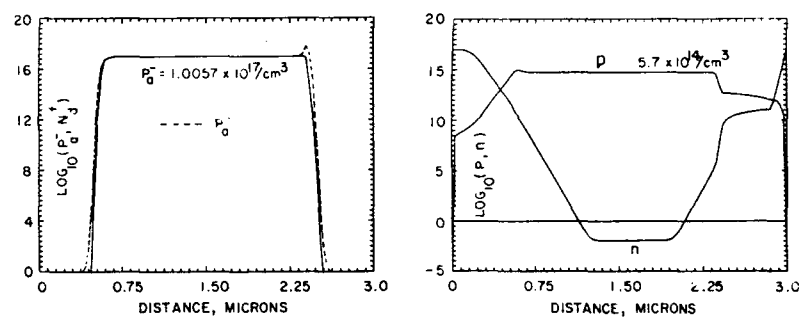


Figure 4. As in figure 3 but for $P_a = 10^{18}$, $N_d = 10^{17}$, at 20v.

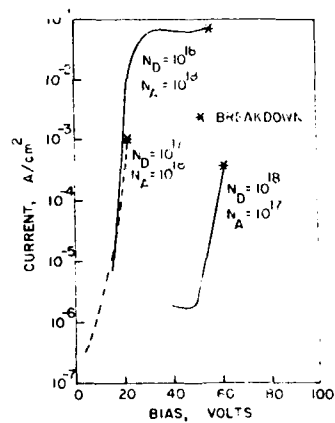


Figure 5. Current voltage characteristics to breakdown for different trap densities.

$N_d(\downarrow)/P_a(\rightarrow)$	10^{18}	10^{17}	10^{16}	10^{15}	10^{14}
0	21 v	25 v	45 v	40 v	28 v
10^{16}	21 v	••	47 v	••	••
10^{17}	21 v	45 v	••	••	••
10^{18}	55 v	62 v	48 v	40 v	30 v
10^{19}	70 v	••	••	••	••

Table 3. Breakdown voltages for different densities of traps.

SUMMARY

The conclusion of this study is that the electrical characteristics of N(LT)N structures are dependent in a very sensitive way on the distribution of traps. The calculations strongly suggest that for N(LT)N structures, the low voltage and high voltage electrical characteristics may provide a signature of the relative density of donor and acceptor traps. Of particular importance is the development of pn [4] junction behavior and low breakdown voltages for acceptor trap dominated material. It is anticipated that the details of the results will depend upon the doping levels of the shallow cladding regions; preliminary studies, however, do not reveal significant qualitative dependencies.

ACKNOWLEDGEMENT

This study was supported by AFOSR.

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CHARACTERIZATION OF ELECTRICAL PROPERTIES OF LOW TEMPERATURE GaAs

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ABSTRACT

LT GaAs(220°C) was grown on an n^+ substrate and capped with n^+ GaAs grown at 600°C (n-i-n). Complete IV and CV measurements were performed. The IV characteristics exhibit ohmic, trap-filling and space-charge-limited regimes. We have developed a model based upon the compensation of background shallow acceptors by deep donor traps, large concentrations of which have been shown to exist in LT GaAs. Computer simulation of the IV curve is compared with experimental results. The "breakdown" is attributed to trap-filling under electron injection. It is also found that when the voltage across the structure is changed, the current takes several seconds to reach steady state. This is consistent with our model, which assumes slow trapping and detrapping in the LT GaAs. High frequency CV measurements show the capacitance to be fairly constant for voltages below "breakdown".

INTRODUCTION

The epitaxial growth of GaAs on a GaAs substrate using molecular beam epitaxy (MBE) is generally conducted at substrate temperatures of approximately 600°C. It has recently been shown, however, that very good epitaxial surface morphology can be obtained using substrate temperatures below 300°C. Slightly conductive in its "as-grown" state, this low temperature (LT) GaAs has been found to become highly resistive upon annealing at temperatures of 500-600°C[1]. One very promising application for this material lies in the area of GaAs IC devices: it has been shown that the inclusion of an (annealed) LT buffer layer between the active region and substrate of a GaAs MESFET reduces the backgating effect, even in the presence of light[2]. In this paper, we report experimental electrical characteristics of LT GaAs and computer simulations which explain the observed electrical behavior of the samples.

EXPERIMENTAL

The test structure is shown in Fig.1. It is basically an n-i-n structure, where i denotes the LT region. AuGe/Ni/Au is used for ohmic contacts. Wet etching through the LT GaAs layer is used for isolation. The n⁺ cap layer is grown at 600°C for 30 minutes, simultaneously annealing the LT GaAs.

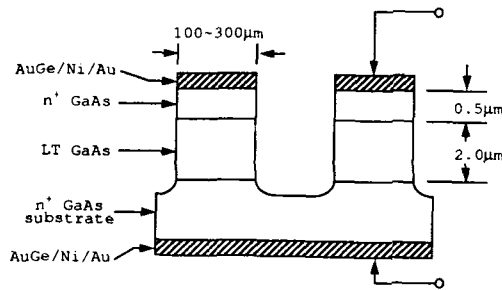


FIGURE 1. Experimental test structure.

Shown in Fig. 2 is a typical i-v curve in log-log scale. The dotted line represents the experimental result. The curve, which is typical of SI GaAs, exhibits three distinct regions: ohmic, trap-filling, and space-charge-limited. The result is thus in agreement with other experiments which indicate a large density of deep traps in LT GaAs[3]. The results of the simulation, given by the solid line, will be discussed in the next section.

IV

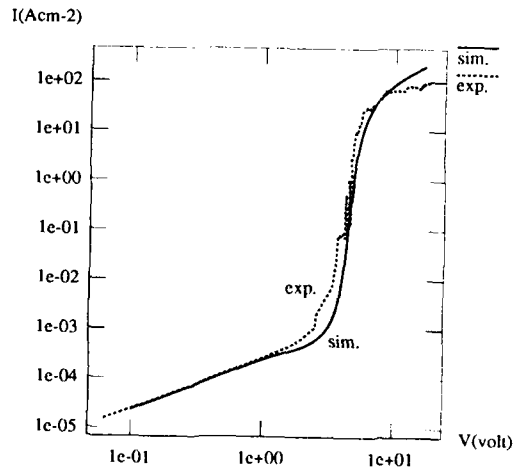


FIGURE 2. Experimental i-v curve and simulation results. Parameters used for simulation are:

$$\begin{aligned}
 N_{dd} &= 2.5 \times 10^{18} \text{ cm}^{-3} \\
 N_a &= 2.5 \times 10^{15} \text{ cm}^{-3} \\
 E_{dd} - E_c &= -0.80 \text{ eV} \\
 \sigma_n &= 1.0 \times 10^{-13} \text{ cm}^2 \\
 \sigma_p &= 2.0 \times 10^{-18} \text{ cm}^2 \\
 B &= 2.0 \times 10^{-10} \text{ cm}^3 \text{ sec}^{-1}
 \end{aligned}$$

In the same experiment, we also observed a slow response of the current to a voltage change. As seen in Fig. 3, when a step voltage is applied, the current requires several seconds to stabilize. Using SRH statistics for recombination through deep traps, and using commonly accepted parameters (electron capture cross section $\sigma_n = 10^{-13} \text{ cm}^2$, deep trap level $E_{dd} - E_c = -0.80 \text{ eV}$) [4], we obtain the electron emission rate $e_n = \sigma_n V_{th} N_t \exp((E_{dd} - E_c)/kT) = 0.3 \text{ sec}^{-1}$, or the time scale $1/e_n = 3 \text{ sec}$. This time scale is in agreement with the result in Fig. 3 (This quantity is not related to either the dielectric relaxation time or the RC constant, both of which are much shorter: $T_{relaxation} = \epsilon\rho = 10^{-5} \text{ sec}$ and $T_{RC} = RC = (pd/A)(\epsilon A/d) = \epsilon\rho = T_{relaxation}$, where $\rho = 10^7 \Omega \cdot \text{cm}$. Note that the speed of LT GaAs optical switches is not limited to 10^{-5} sec , because under high optical carrier injection the resistivity ρ is much smaller). To assure that every point in the i-v curve shown in Fig. 2 is at steady state, we waited about 10 seconds each time the applied voltage was stepped up or down before taking the current measurement.

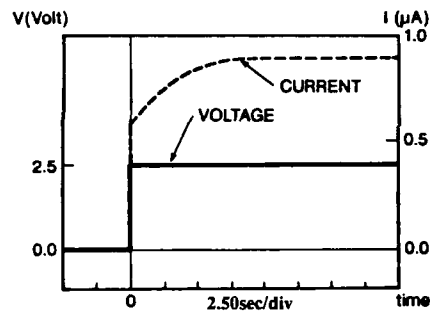


FIGURE 3. Transient due to slow trapping-detrapping process in LT GaAs.

C-V measurements were also performed. The curve is generally flat. However some of the samples exhibit a dip at low voltage as shown in Fig. 4. The significance of this feature is not yet determined.

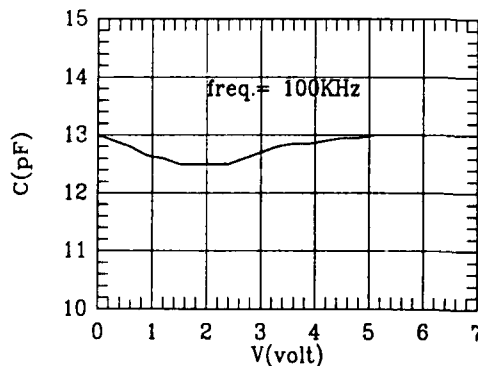


FIGURE 4. C-V measurement.

SIMULATIONS

In an effort to gain insight into the conduction mechanism in LT GaAs, we have performed computer simulations of its current-voltage (i-v) characteristics. Three nonlinear equations (Poisson equation and continuity equations for electrons and holes) must be solved simultaneously [4]:

$$\frac{d^2\Phi}{dx^2} = -\frac{q}{\epsilon} (p - n - N_a + N_{dd}^*) \quad (1)$$

where N_a is the density of shallow acceptors, and N_{dd}^* is the density of ionized deep donors.

$$\frac{dJ_p}{dx} = q(G - R), \text{ where } J_p = -q\mu_p p \frac{\partial\Phi}{\partial x} - qD_p \frac{\partial p}{\partial x} \quad (2)$$

$$\frac{dJ_n}{dx} = -q(G - R), \text{ where } J_n = -q\mu_n n \frac{\partial\Phi}{\partial x} + qD_n \frac{\partial n}{\partial x} \quad (3)$$

Direct recombination and SRH recombination are taken into account. The rate of direct recombination is given by

$$G - R = -B(np - n_i^2) \quad (4)$$

SRH statistics are used to model recombination through deep trap levels.

$$N_{dd}^* = \frac{e_n + c_p p}{e_n + e_p + c_n n + c_p p} N_{dd} \quad (5)$$

$$G - R = -\frac{pn - \frac{e_n e_p}{c_n c_p}}{\frac{1}{c_p N_{dd}} \left(n + \frac{e_n}{c_n} \right) + \frac{1}{c_n N_{dd}} \left(p + \frac{e_p}{c_p} \right)} \quad (6)$$

where e_n and e_p are respectively electron and hole emission rates; c_n and c_p are respectively electron and hole capture coefficients.

The finite difference method is used to solve the problem numerically. Each point on the grid is associated with three unknowns, Φ , Φ_n and Φ_p , which are the electrostatic potential, electron Fermi level and hole Fermi level respectively. The differential equations are first discretized into difference equations [5]. Multidimensional Newton-Raphson iteration is then used to find the solution.

The simulation result, as already shown in Fig. 2, fits well with experimental result. The values of electron and hole capture cross sections are taken from EL2 traps in SI GaAs [4].

Fig. 5 shows the band diagrams at thermal equilibrium and at an applied voltage of 2 volts. From the band diagram, the distribution of empty (ionized) deep trap density and the inverse of free electron density under various biases are calculated, as shown in

Fig. 6. Curves of empty deep trap density and of the inverse of free electron density have the same shape, so they are shown in the figure as one curve. The region under the curves in Fig. 6 is highly resistive, because there are few free electrons there, and deep traps are not completely filled.

When the applied voltage is low, this region is wide and highly resistive, and conduction is ohmic. When the bias is increased, more electrons are injected into LT GaAs from the cathode, filling more deep traps and increasing the free electron density. Thus the highly resistive region gradually shifts toward the anode, becoming narrower and less resistive, which can be seen in Fig. 6. A dramatic current increase, which is commonly referred to as "breakdown", occurs when this region is about to disappear. Current is solely limited by space charge when this resistive region vanishes completely; this regime is thus called space-charge-limited.

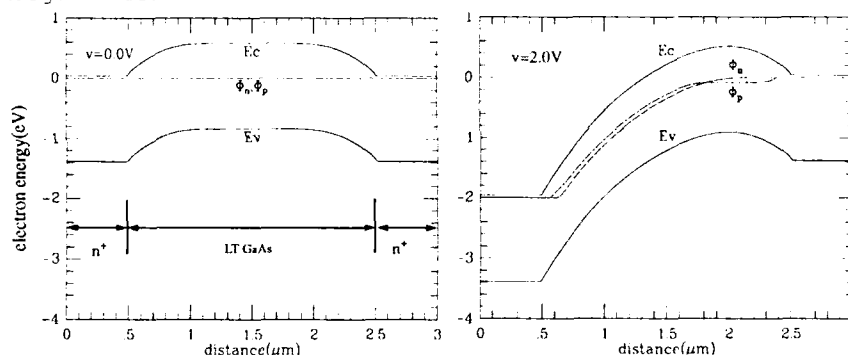


FIGURE 5. Band diagram at thermal equilibrium and under 2volt bias.

Note that the capacitance shown in Fig. 4 is equivalent to that of a parallel-plate capacitor with a separation of $1.2\mu\text{m}$, and this distance is roughly the width of the highly resistive region shown in Fig. 6. This can be explained by the fact that when a small AC voltage is applied to the n-i-n structure, the modulation of charges occurs mainly at the edges of this region.

SUMMARY

We measured the electrical properties of LT GaAs using an n-i-n structure. The i-v curve showed three distinct regions. We also observed slow trapping-detrapping of electrons with a time scale of 1-10 seconds. These results can be well explained by a model which is based upon the compensation of shallow acceptors ($\sim 10^{15}\text{cm}^{-3}$) by deep donor electron traps ($\sim 10^{18}\text{cm}^{-3}$). We believe this model can

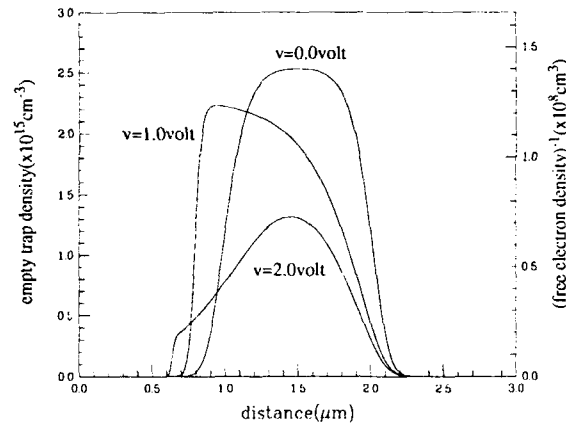


FIGURE 6. Empty deep trap density and the inverse of free electron density.

further be used in simulations of electrical device structures which incorporate LT GaAs.

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The authors would like to acknowledge the support of staffs of microfabrication laboratory and device characterization laboratory, University of California at Berkeley.

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EFFECT OF GROWTH CONDITIONS ON OPTICAL RESPONSE OF GaAs GROWN AT LOW SUBSTRATE TEMPERATURE BY MBE

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ABSTRACT

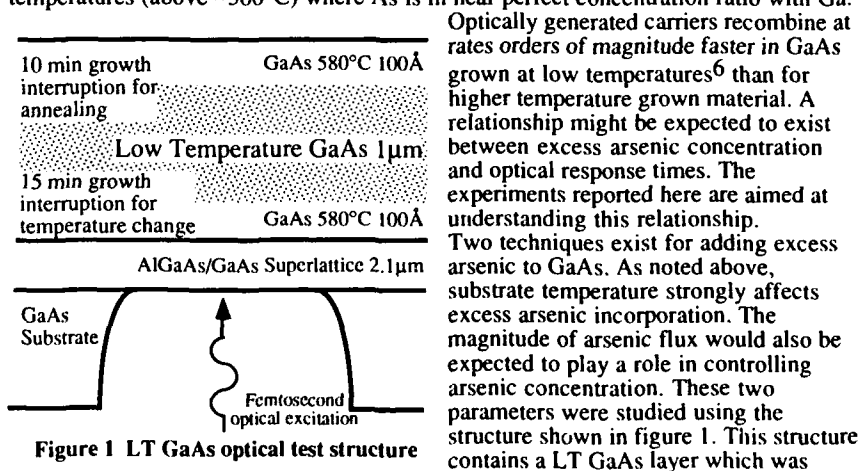
The effect of growth conditions on the properties of GaAs grown by molecular beam epitaxy at low substrate temperatures has been studied. It has been found that the response time to 100 fsec 830nm light pulses is a function of substrate temperature and arsenic flux. The reason for variation of optical response with growth conditions is related to the nature of the incorporation of excess arsenic. A recent model proposed by Warren and others is invoked to explain the change in optical response with growth conditions. Further substantiation of this model comes from experiments on the annealing of low substrate temperature GaAs which has been doped with silicon.

INTRODUCTION

The applications of Low substrate Temperature GaAs (LT GaAs)¹ grown by molecular beam epitaxy (MBE) exploit its properties of high resistivity², high breakdown voltages³ and fast optical response⁴. Applications for materials with fast optical response include the generation of THz frequency signals from subpicosecond optical pulses. The maximum frequencies which can be obtained are limited by recombination time of carriers following optical excitation. The study reported here has two purposes. First, the effect of growth conditions on optical response has been examined to determine the conditions leading to the fastest optical response. Second, this data has been analyzed to learn more about the nature of the recombination process and the role that excess arsenic plays in this process. The nature of excess arsenic incorporation following annealing is studied through electrical characterization.

EXPERIMENTAL

Excess arsenic incorporation in GaAs grown at low substrate temperatures (~200°C)⁵ is an unusual phenomena when compared to the properties of GaAs grown at high temperatures (above ~300°C) where As is in near perfect concentration ratio with Ga.



Optically generated carriers recombine at rates orders of magnitude faster in GaAs grown at low temperatures⁶ than for higher temperature grown material. A relationship might be expected to exist between excess arsenic concentration and optical response times. The experiments reported here are aimed at understanding this relationship. Two techniques exist for adding excess arsenic to GaAs. As noted above, substrate temperature strongly affects excess arsenic incorporation. The magnitude of arsenic flux would also be expected to play a role in controlling arsenic concentration. These two parameters were studied using the structure shown in figure 1. This structure contains a LT GaAs layer which was

grown under different substrate temperatures and arsenic overpressures. The LT GaAs was grown on a superlattice buffer of 290Å $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$ / 10Å GaAs, repeated 70 times, which isolates the LT GaAs layer from substrate defects and impurities, and serves as an optically transparent etch stop for etching observation holes from the back of the substrate. The motion of arsenic precipitates which result from excess arsenic in the LT GaAs layer will also be stopped by this layer. Thus, the properties of the region being examined can be ascertained without the possibility of unintentional modification of surrounding layers and the difficulties in analysis of signals from multiple regions of the structure.

Growth and anneal of the LT GaAs was observed by reflection high energy electron diffraction (RHEED). All low temperature GaAs layers exhibited polycrystalline RHEED reconstruction patterns at the end of their growth. The onset of the polycrystalline pattern was a function of substrate temperature. Lower substrate temperatures resulted in earlier observation of the change in pattern. Annealing the samples at 580°C returned the RHEED pattern to single crystal reconstruction, except for the sample grown at 180°C which remained polycrystalline. Samples were analyzed by optical transient absorption spectroscopy at the band-edge to directly determine carrier dynamics.

Femtosecond continuum pump-probe spectroscopy techniques were performed using 100 fsec optical pulses 10 nm wide centered at 830nm. for excitation. The injected carrier density was estimated to be 10^{17} cm^{-3} . The probe consisted of the 760-880 portion of the pump continuum. Differential transmission spectrum (DTS) were accumulated on an optical multichannel analyzer (OMA).

Differential transmission spectrum are seen in figures 2a and 2b for LT GaAs grown at 200°C at an arsenic beam flux pressure of $8 \times 10^{-6} \text{ T}$. The baselines of curves for each period of time are offset for clarity. Initial hole burning at the pump wavelength due to preferential state filling and fast relaxation to the band edge is seen. Following initial filling of the bands at 830nm, carriers relax in energy down to 860nm (1.442 eV) within 300 fsec. The apparent band edge 1.44 eV, is blue shifted from the normal GaAs band edge. The cause of the blue shift is not known. Strain due to excess arsenic

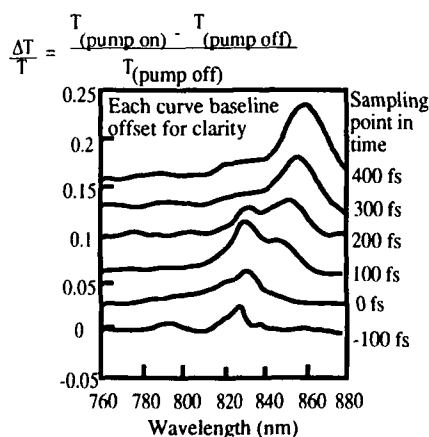


Figure 2a DTS spectrum to 400 fs

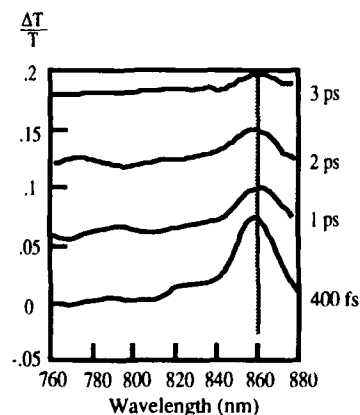


Figure 2b DTS spectrum from 400fs to 3 ps

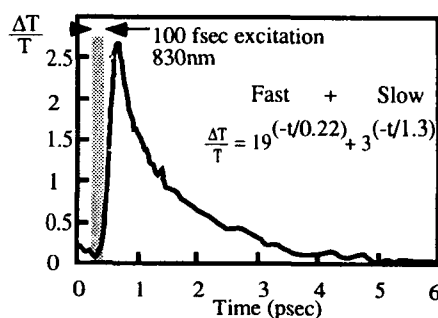


Figure 3 Transmission decay at 860nm

causing an increase in lattice constant would be expected to result in red shift. Strain from the AlGaAs window layer beneath the LT GaAs where the substrate has been removed may shift the bandgap and cause the blue shift.

Observations of the absorption response at a single wavelength is seen in figure 3. The change of absorption at 860nm is shown as a function of time. There are fast and slow components to this response which can be analyzed as a sum of two exponentials - each with amplitude as well as time constant. For efficient THz generation, the fast portion

of the decay would be desired to be the largest, if not the sole component amplitude.

For all growth conditions studied, the amplitude of the fastest component was more than 5 times larger than the amplitude of the slower component. The decay time constant of the faster component is plotted as a function of substrate temperature in figure 4. Decay time falls with substrate temperature until the substrate temperature is lowered to the point where thick GaAs cannot be grown before the onset of polycrystalline growth. 180°C grown GaAs was almost entirely polycrystalline. Growth at 190°C and 200°C resulted in thin polycrystalline layers at the surface.

In addition to fall in decay times with substrate temperature, resistivity and arsenic concentration are known to increase. As will be discussed, these observations are consistent with a Schottky barrier Fermi level pinning model. The excess arsenic might be thought to contribute to an increase in the magnitude of the mechanism responsible for faster recombination times. A series of growths as a function of arsenic pressure were grown at 200°C. These structures are also dominated by the amplitude of the fast decay component. The variation of decay time with arsenic pressure is seen in figure 5.

Decay time falls with arsenic pressure. This result does not seem to be consistent with the effects of lowering substrate temperature where arsenic concentration is known to increase. Despite the likelihood that increased arsenic incorporation results from increased arsenic flux, the fall in decay times seems to indicate that there is more than simple presence of arsenic responsible for faster recombination times. The nature of

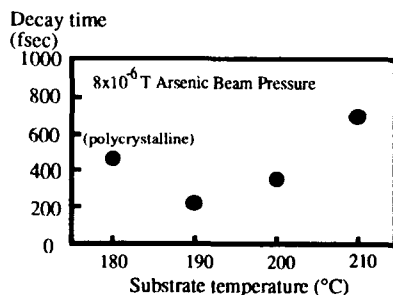


Figure 4 Fast component decay time versus substrate temperature

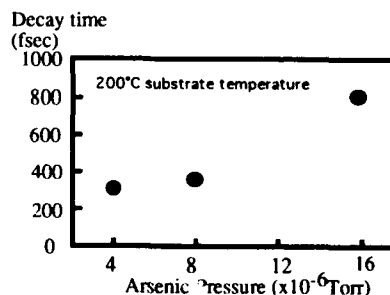


Figure 5 Fast Component decay time versus arsenic pressure

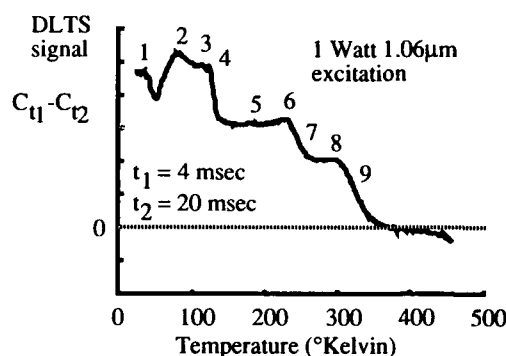


Figure 10 Optical DLTS spectrum for LT GaAs

Deep level transient spectroscopy (DLTS) measurements were performed on the conducting samples. A boxcar plot from the optical excitation DLTS measurement of one sample grown at 200°C, 8×10^{-6} T As pressure, and annealed at 850°C is seen in figure 10. The sign of the measured DLTS signal indicates hole trap emissions. Analysis of boxcar plots with different rate windows indicates the characterization of common hole traps not commonly seen in GaAs. There are two known DLTS boxcar spectrum which resemble this spectrum which are

not the result of a number of discrete deep levels. The first is electron trapping, rather than hole emission, in AlGaAs by the DX center. This type of signature has also been seen in polycrystalline GaAs grown on an oxide by MBE.

Annealing reduces the magnitude of the DLTS signal indicating a reduction in deep level concentration with annealing. None of the samples showed evidence of electron traps to concentrations greater than 10^{16} cm^{-3} which was the limit due to the presence of hole polarity signals. Electrical excitation DLTS measurements were also performed to look specifically for electron traps in these n-type samples. There were no electron traps seen down to the 10^{15} cm^{-3} detection limit. If EL2 is present in the annealed material, the concentration must be very small.

All of the experiments conducted are consistent with the nature of arsenic precipitates acting as buried Schottky barriers and not some simple form of deep level. The insulating nature of silicon doped LT GaAs can be explained by arsenic precipitates acting as spherical Schottky barriers with overlapping depletion regions⁷. Arsenic precipitates become more widely dispersed as arsenic dissolves into the crystal. For proper spacing and doping concentrations, the Schottky depletion regions no longer overlap. The relation between optical response and arsenic precipitates can be explained by recombination at precipitates.

Assuming a geometry of 40Å diameter arsenic precipitates separated by 200Å, the furthest separation (greatest distance for an electron to travel to recombine at a precipitate), is $\sqrt{3} \times 200\text{Å}$.

Assuming thermal velocities:

$$v_T = \sqrt{\frac{kT}{2\pi m^*}} \quad k = \text{Boltzman const, } T = \text{temperature, } m^* = \text{effective mass}$$

$$= 1.04 \times 10^7 \frac{\text{cm}}{\text{sec}} \quad (\text{electrons}); \quad = 0.4 \times 10^7 \frac{\text{cm}}{\text{sec}} \quad (\text{holes})$$

Electrons first recombine at arsenic precipitates (assuming p type background conductivity) taking:

$$\frac{\sqrt{3} \times 2 \times 10^{-6} \text{ cm}}{1.04 \times 10^7 \frac{\text{cm}}{\text{sec}}} = 333 \text{ fsec}$$

580°C	100 Å	$1 \times 10^{18}(\text{cm}^{-3})$
580°C	100 Å	undoped
200°C	5000 Å	Si doped
580°C	1000 Å	undoped
GaAs substrate		

Figure 6 Doped LT GaAs

excess arsenic in the crystal due to higher arsenic flux seems to be different.

An alternative technique to alter the nature of excess arsenic in the crystal lattice is through post growth annealing. Annealing is necessary for formation of arsenic precipitates which are thought to be responsible for localized Schottky barriers. The properties of LT GaAs annealed at different temperatures is studied using the structures seen in figure 6. GaAs with varying silicon

doping concentrations is grown at 200°C and annealed at 750°C, 850°C and 950°C. A summary of room temperature photoluminescence (PL) measurements is seen in figure 7. The PL intensity is a function of doping concentration and annealing temperature. The undoped samples do not show significant PL for the annealing conditions studied. Free carrier densities measured by Hall measurements for doped samples is seen in figure 8. The Hall mobilities for these samples are seen in figure 9. Free carrier density increases with annealing temperature. Mobility also increases with anneal temperature.

Both observations could result from decrease in concentration of centers responsible for compensation or scattering as a result of annealing. The buried Schottky barrier model, however is also consistent with these observations. The distribution of arsenic precipitates could be altered by annealing to distributions predicted by Warren to result in varying magnitudes of conductivity. If, on the other hand, the conductivity was being compensated by centers which were removed by annealing, some fraction of these centers would be easily measurable by DLTS.

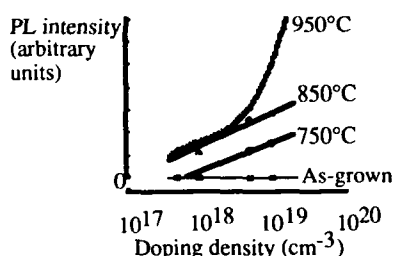


Figure 7 PL intensity as a function of doping density and post growth anneal temperature

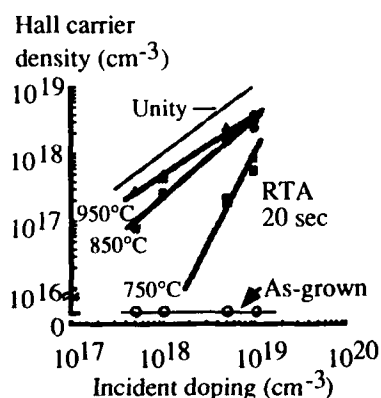


Figure 8 300°K electron density vs incident doping as a function of anneal

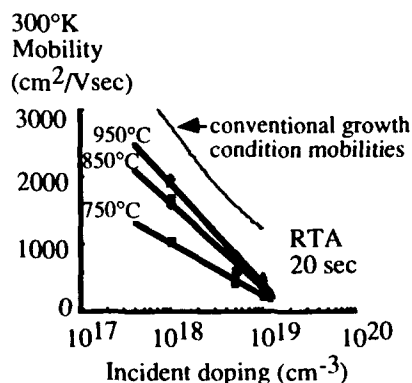


Figure 9 300°K Hall mobility vs incident doping as a function of anneal

An electric field is then established $E = \frac{q}{4\pi\epsilon_0}$ which causes holes to migrate to arsenic inclusions with a rate of $\frac{1 \times 10^{-6} \text{ cm} \times \sqrt{3}}{1.85 \times 10^6 \frac{\text{cm}}{\text{sec}}} = 940 \text{ fsec}$.

These figures approximate actual decay time constants observed. Small changes in precipitate geometries could be applied to bring these values closer to those observed. This model would indicate that increased arsenic precipitate concentrations would be needed for faster recombination times. The substrate temperature dependence of recombination time would support this dependence of decay times on arsenic concentrations. The explanation of decay time variation with arsenic pressure is not so easily explained. Arsenic precipitate density would have to increase with decrease in arsenic pressure. The mechanism for such behavior is not known.

CONCLUSIONS

LT GaAs has recombination times which are a function of growth conditions. A simple model of recombination at arsenic precipitates acting as Schottky barriers is consistent with the substrate temperature dependence of decay times. The Schottky barrier model to explain arsenic precipitates is further supported by annealing of Si doped LT GaAs subject to post growth annealing. DLTS measurements fail to find a deep level, or levels which exist following rapid thermal annealing. The existence of significant concentrations of any such level prior to annealing seems likely to be small. A better understanding of the nature of arsenic precipitate formation is needed to further test this model, and to optimize the growth of LT GaAs for obtaining the fastest switching performance.

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DEFECTS IN LOW-TEMPERATURE-GROWN MBE GaAs AS STUDIED BY A VARIATION OF TSC SPECTROSCOPY

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ABSTRACT

A zero-bias thermally stimulated current (TSC) spectroscopy under both optical (1.96eV) and electrical excitation using samples with a Schottky contact on the top was applied to annealed LTMBE GaAs grown at different temperatures, and bulk SI GaAs with different stoichiometries. The results show that: 1) the new TSC technique is capable of revealing the traps at $235\text{K} < T < 380\text{K}$ and is effective in indicating the crystal stoichiometry of bulk SI GaAs; 2) the driving force for the currents under a zero-bias comes from the built-in surface field as well as a thermal gradient; 3) the trap species in the annealed LTMBE GaAs samples and the annealed control SI GaAs sample are similar, especially for $T_1(0.79\text{eV})$, $T_2(0.33\text{eV})$, $T_3(0.29\text{eV})$, and $T_4^*(0.16\text{eV})$; and 4) the trap densities in LTMBE samples are higher than those in the control samples and are dependent on the MBE growth temperature.

1. INTRODUCTION AND EXPERIMENTAL TECHNIQUE

Molecular-beam-epitaxial (MBE) GaAs is normally grown at temperatures of 580°C – 600°C and at these temperatures it is relatively routine to attain shallow donor and acceptor concentrations in the 10^{14}cm^{-3} range and an even smaller concentration of electron and hole traps. In a clean MBE system using proper growth conditions and pure arsenic, essentially trap free GaAs can be grown [1]. Recently, however, Smith et al. showed that MBE GaAs grown at 200°C had much different properties and that when used as a buffer layer could remarkably improve some critical characteristics of GaAs MESFET devices [2]. The outstanding characteristic of low-temperature-grown MBE (LTMBE) GaAs is a large excess of As (1-2%), which leads to a deep donor (As_{Ga} -related) concentration of more than 10^{19}cm^{-3} , and after a 600°C anneal, large (60\AA), dense (10^{17}cm^{-3}) precipitates of As, accompanied by the formation of a high resistivity phase of the material [3-5]. The anneal could be either an in-situ anneal in the MBE growth chamber or a furnace/rapid thermal anneal in an extrinsic apparatus. To elucidate the mechanism of the transition from the conductive phase to the high resistive phase by the anneal, more information about the deep centers in the annealed LTMBE GaAs material is needed.

The regular thermally stimulated current (TSC) spectroscopy has proven to be very useful in revealing the deep centers in bulk liquid encapsulated Czochralski (LEC) semi-insulating (SI) GaAs and in studying the metastable traps associated with the transition from the normal state of EL2 to its metastable state in SI GaAs [6,7]. However, the large dark currents in the annealed LTMBE GaAs tend to mask the TSC peaks, especially those peaks at high temperatures, although several deep centers in the material were observed by means of subtraction and normalization methods [8]. In this paper, we use a variation of the TSC technique, i.e. zero-bias TSC (ZBTSC) using samples with a Schottky contact on the top and a surface absorbed light (1.96eV), and apply it to annealed LTMBE GaAs grown at different temperatures from 200 to 400°C . A similar technique has been introduced by others [9]. For a better understanding of the LTMBE traps, we carry out measurements on the original substrate material and several other SI GaAs samples with different stoichiometries.

The sample structure and the schematic diagram used for both regular TSC and ZBTSC measurements are shown in Fig.1. A sandwich structure ($6 \times 6\text{ mm}^2$ in

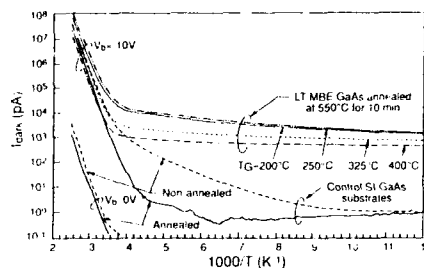
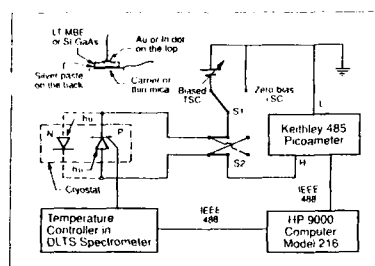


Fig.1 Sample structure and schematic diagram for various TSC. Fig.2 Arrhenius plots of I_{dark} 's with -10V & 0V biases for samples.

size) with a small thermally evaporated Au or In Schottky contact (diameter of 0.7 or 1.2 mm) on the top and silver paste on the back was used to study the dark current (I_{dark}), the photocurrent (I_{ph}), and the TSC current. The above band-edge excitation light of 1.96eV was provided from a 1.5mW He-Ne laser. In the ZBTSC measurements, the sample was rapidly cooled from 380K down to 81K (within 9 min.) with a bias, which could be varied between negative and positive values by changing the polarity of the sample. The bias was supplied from batteries or the power supply in a DLTS spectrometer. After the sample was illuminated at 81K for 5 min. the switch S1 was switched to the right for a zero bias and the thermal scan started with a heating rate of 0.3K/s. The switch S2 was set to keep the same connection between the sample and the picoammeter in the ZBTSC measurements; i.e. for the positive bias case represented by solid lines, S2 was set towards the right and for the negative bias case represented by dashed lines, towards the left. It should be pointed out here that the ZBTSC with a bias but no light excitation during the cooling cycle, and without light excitation at 81K, can also reveal traps at $T > 235\text{K}$, which is referred to as "electrically-excited ZBTSC" to differentiate the "optically excited ZBTSC" mentioned above. Both a digital electrometer (Keithly 616) and an autoranging picoammeter (Keithly 485) were used at various times in the biased TSC and ZBTSC measurements, but the ZBTSC spectra reported in this paper were measured by the latter instrument.

The four LTMBE GaAs samples used in this study were grown on consecutive LEC SI GaAs substrates in a Varian GEN II system under normal As stabilized conditions using As_2 . The growth temperature was varied from 200 to 400°C and the thickness of each MBE layer was 2 μm . Post-growth anneal for the samples was subsequently performed under a GaAs proximity wafer at 550°C for 10min. in a flowing inert gas. One of two LEC SI GaAs control samples was annealed in this same way. Also studied were three LEC SI GaAs samples with different crystal stoichiometries, i.e. As-rich, Ga-rich, and more Ga-rich. Their detailed properties can be found in Refs. 6 & 8, but all were ingot-annealed at 950°C.

2. RESULTS AND DISCUSSION

The Arrhenius plots of I_{dark} under a negative bias (-10V) for four annealed LTMBE GaAs and two control LEC SI GaAs samples (with In Schottky contacts), and under a zero bias (S1 towards right) for the latter two samples are shown in Fig.2. From the figure it can be seen that: 1) under a bias of -10V, the I_{dark} 's at $T < 200\text{K}$ in the annealed LTMBE GaAs are about three orders of magnitude higher than the I_{dark} in the annealed control SI GaAs and the I_{dark} 's at $T > 300\text{K}$ in both samples are dominated by an activation energy of about 0.78eV; 2) the I_{dark} 's in annealed LTMBE GaAs are closely related to the growth temperature, i.e. for higher T_0 , I_{dark} is lower (note that I_{dark} for the 200°C LTMBE sample was obtained after the sample cleaved during the rapid cooling cycle); 3) as compared to the non-annealed control sample (NCS), the

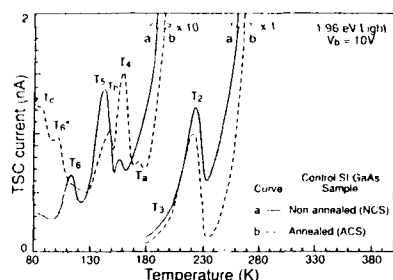


Fig. 3 Comparison of traps in two control SI GaAs samples.

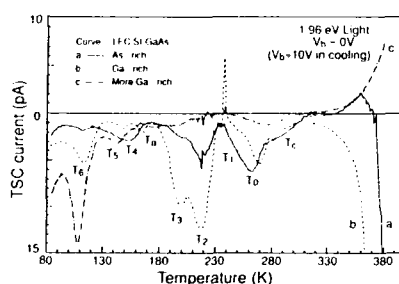


Fig. 6 Spectra of ZBTSC(0) for three LEC SI GaAs samples.

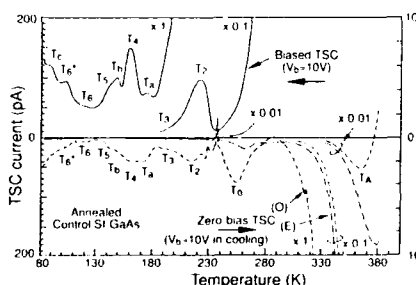
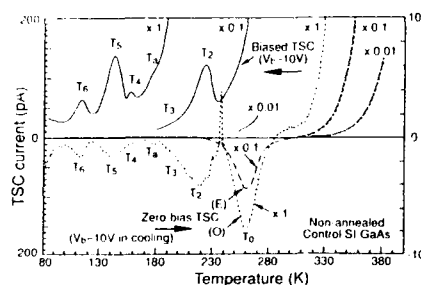


Fig. 4 & 5 Comparison of regular TSC and ZBTSC (E & O) for two control samples

annealed control sample (ACS) shows lower I_{dark} , especially in the temperature range $140\text{K} < T < 250\text{K}$, which suggests defect or impurity modifications induced by the annealing; and 4) I_{dark} can be measured under a zero bias for the control samples and annealed LTMBE samples as well (not shown in the figure) with nearly the same activation energy as that under a bias of -10V . This last fact suggests a small (mV) offset voltage, possibly in the ammeter, which will produce a small equilibrium I_{dark} and be a limiting factor in the ZBTSC.

The traps in the two control samples were first compared by the regular (or biased) TSC method, as shown in Fig. 3. In the figure, two changes caused by the anneal can be found: 1) an increase in T_4 and T_6^* , and a decrease in T_2 and T_5 ; and 2) the appearance of new TSC peaks, T_0 and T_c . Similar changes, especially the increase of T_4 and T_6^* , were found in electron-irradiated SI GaAs using samples with In ohmic contacts and 1.46eV light, an almost penetrating light at $T < 90\text{K}$ [10]. The similarity between the electron-irradiated and the annealed SI GaAs is helpful in understanding the role of annealing in making SI GaAs more resistive, as will be discussed later.

Comparisons of regular TSC and ZBTSC with both electrical excitation (E) and optical excitation (O), and with a bias of $+10\text{V}$ during the cooling cycle, are shown in Figs. 4 & 5 respectively, for the two control samples. From the two figures it can be seen that: 1) in comparison with the regular TSC spectra, the ZBTSC(0) spectra reveal nearly the same TSC peaks at $T < 235\text{K}$, but more TSC peaks, T_0 and T_c (only in the ACS) at $T > 235\text{K}$; 2) at high temperatures, the ZBTSC(E) spectra reveal nearly the same TSC peaks (T_0 and T_c) as the ZBTSC(O), but with larger peak heights and some shift in the peak positions; and 3) a spike structure at $T \approx 235\text{K}$ appears in the spectra of both ZBTSC(E) and (O), but does not appear in the regular TSC spectra, perhaps due to masking by the large dark currents. Note that the spectral differences between two control samples are not only present at low temperatures, but also at high temperatures, i.e. the negative currents and the appearance of T_c in the ACS and the positive currents and the absence of T_c in the NCS.

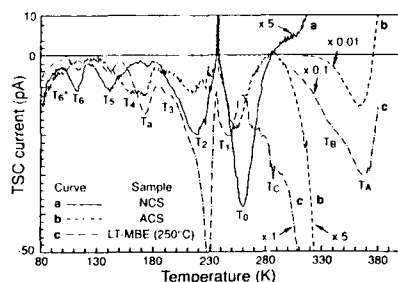


Fig.7 Comparison of ZBTSC(0) for a LTMBE and NCS/ACS samples.

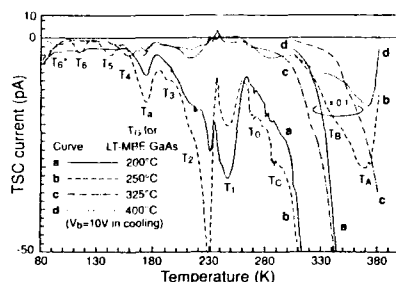


Fig.8 Comparison of ZBTSC(0) for four LTMBE GaAs samples.

The defects in LEC SI GaAs grown under different melt stoichiometries have been well studied by the regular TSC technique using samples with either ohmic contacts [6] or Schottky contacts [8]. It is found that the relative peak height ratios of T_0/T_1 , T_2/T_3 , and T_5/T_6 are strongly dependent on the crystal stoichiometry, i.e. the stoichiometry transition from Ga-rich to As-rich favors the occurrence of traps T_0 , T_2 , and T_5 . The ZBTSC(0) spectra (with a bias of +10V during the cooling cycle) on the same samples, with Au Schottky contacts, as shown in Fig.6, indicate the same stoichiometric dependence as determined by the T_0/T_1 , T_2/T_3 , and T_5/T_6 ratios. In addition to T_1 , the spectra at high temperatures show some differences in the signs of the currents, i.e. negative currents for the Ga-rich sample, positive currents for the more Ga-rich sample, and a change in the current sign for the As-rich sample, resulting in a positive peak at about 360K. This peak occurs at a temperature near that expected for EL2. An interesting observation is the difference in the amplitudes of the spike features at 235K, i.e., the strongest spike is in the Ga-rich sample, whereas the weakest spike is in the As-rich sample.

We next apply ZBTSC(0) to the annealed LTMBE GaAs samples grown at temperatures of 200, 250, 325, and 400°C. For comparative purposes, the spectrum of ZBTSC(0) for the 250°C LTMBE sample is shown in Fig.7 together with those for the two control samples. The figure shows that in the LTMBE sample: 1) at $T < 235$ K almost the same trap species as those found in the two control samples can be observed, i.e. T_2 , T_3 , T_4 , T_5 , T_6 , and T_7^* (T_7^* appears in the 325°C LTMBE sample, see Fig.8); 2) at $T > 235$ K, in addition to T_1 (which only appears in the annealed control sample), more trap species can be found, i.e. T_0 , T_2 , T_3 , T_4 , T_5 , T_6 , and T_7 ; and 3) the traps have much higher densities than those in the control samples, as can be seen by normalizing to the respective I_{ph} 's at 81K (5.6nA, 70nA, and 550nA for the 250°C LTMBE, the ACS, and the NCS, respectively). Using an approximate equation $E_t = kT_m \ln T_m^4 / \beta$, where E_t is the trap depth, k Boltzmann's constant, T_m the TSC peak temperature, and β the heating rate for the thermal scan, the T_m 's and E_t 's for the traps in the 250°C LTMBE sample are T_0 (370K, 0.79eV), T_2 (340K, 0.72eV), T_3 (286K, 0.59eV), T_4 (268K, 0.55eV), T_5 (246K, 0.49eV), T_6 (215K, 0.43eV), T_7 (193K, 0.37eV), T_1 (173K, 0.33eV), T_4 (158K, 0.29eV), T_5 (142K, 0.26eV), T_6 (113K, 0.20eV), and T_7 (95K, 0.16eV). In the ACS we also have T_2 (88K, 0.15eV). The spike feature at 235K appears in the LTMBE sample just as in two control samples, and seems to be related to a sudden change in defect properties, perhaps driven by the charge transfer during emission. Since there is no change in the spike position with changing heating rate, the feature is not a normal TSC peak.

A comparison of the ZBTSC(0) spectra for four LTMBE GaAs samples grown at different T_0 , but annealed under the same conditions, are shown in Fig.8, and indicate that: 1) the LTMBE GaAs samples each contain nearly the same trap species (T_0 through T_7^*); and 2) the peak heights of the TSC peaks show dependency on T_0 , i.e., the lower the T_0 , the higher the trap densities (the lower peak heights in the 200°C sample than in the 250°C sample may be due to the lower I_{ph} at 81K and the lower carrier lifetime in the former sample).

To understand the driving force for the dark current and TSC under a zero bias, the spectra of ZBTSC(E) and ZBTSC(O) for a bulk LEC SI GaAs sample (Ga-rich), are presented in Figs. 9a & 9b, respectively. The spectra were taken by using different biases from -5V to 10V during the cooling cycle. The figures show that: 1) the spectral structures of both ZBTSC(E) and ZBTSC(O) are varied by changing the bias; and 2) the variations of the TSC peaks are not only seen in the peak heights, but also in the peak directions. The spectral differences between ZBTSC(E) and ZBTSC(O) include the following: 1) there is no TSC feature at $T < 235\text{K}$ for ZBTSC(E); and 2) the two TSC peaks in ZBTSC(E), i.e., T_0 (a negative peak) and T_1 (a positive peak), are much larger than those in ZBTSC(O) (T_1 appears only as a shoulder due to the appearance of T_2 in the ZBTSC(O) spectra). These facts must be considered in relationship to the possible driving mechanisms for the zero-bias current, which include an offset voltage in the ammeter, a temperature difference between the contacts [9], or a non-equilibrium Fermi level due to trap filling during the cool-down phase. An offset voltage would produce peaks in the same direction for both electron and hole emission, which is certainly not observed in Figs. 9a & 9b. A temperature differential would produce opposite peak directions for electron and hole emission [9], respectively, but in Fig. 9b it appears that some of the peaks, such as T_3 , are negative for some cooling conditions and positive for others. To explain this effect it may be necessary to invoke the third mechanism, namely, a different non-equilibrium Fermi level dependent on cooling conditions. In a dark SI GaAs crystal, surface band bending should be small, because the Fermi level is near mid-gap in the bulk, and is usually thought to be pinned near mid-gap at the surface, also [11]. The surface potential, however, can easily be modified by carrier injection and subsequent trapping at surface states, and the resulting non-equilibrium surface field will persist at low temperatures since the carriers cannot be re-emitted. Since the equilibrium band bending is small to begin with, as explained earlier, a relatively small change in the surface potential could actually change the direction of the surface field. The bias polarity and presence or absence of light during cooling would be important here, because the relative numbers of injected electrons and holes would determine the final surface potential. Since the surface traps are deep, the non-equilibrium surface field would persist as the sample warmed up, perhaps even to 400K. We believe this mechanism could explain many of the unusual features of our ZBTSC spectra. For example, in Fig. 9a we would suggest that a negative bias (without light) would inject electrons, filling some deep electron traps at the surface as well as a shallower bulk trap T_1 , which emits at 254K. A positive bias, on the other hand, would inject holes, filling deep hole traps on the surface and thus changing the surface field direction, and also filling a bulk hole trap T_0 (at 268K) as well as possibly another hole trap emitting near 380K. The ZBTSC spectra may well be influenced by a temperature differential also, but we believe that this mechanism alone is not sufficient to explain all of the data.

As to the nature of the TSC traps in LTMBE GaAs, none have been positive-

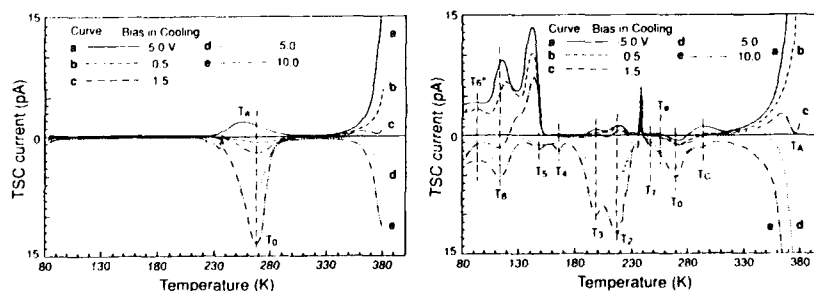


Fig. 9a & 9b Spectra of ZBTSC (E & O) for a bulk sample (bias from -5V to 10V).

ly identified at this time but some of the trends are interesting. First of all, the samples grown at the lower temperatures, 200 & 250°C, appear to have a much richer trap spectrum than those grown at 325 & 400°C. This fact agrees with the known greater As richness of the 200 & 250°C samples, and much greater As_{Ga} concentrations. Secondly, many of the same traps appear in LTMBE GaAs as are found in SI GaAs and electron-irradiated (EI) GaAs. For example, the traps $T_4(0.29\text{eV})$ and $T_5(0.33\text{eV})$ are close in energy to the EI defect E3(0.29eV) which is known to be an As-sublattice defect. Also, $T_6(0.20\text{eV})$, $T_6^*(0.16\text{eV})$, and $T_7(0.15\text{eV})$ are close to the EI defect E2(0.15eV), which is known to be related to V_{As} . Finally, the most highly concentrated defect $T_A(0.79\text{eV})$ has an energy close to the DLTS value for EL2(0.82eV) which is known to be related to As_{Ga} . Since high As_{Ga} concentrations have been found in LTMBE GaAs by other techniques, it is tempting to associate T_A with As_{Ga} also. Although further studies, perhaps to higher TSC temperatures, will have to be carried out before T_A can be completely characterized, still it should be noted that this center can not be observed at all with regular TSC so that the ZBTSC is necessary.

In summary, the defects in the bulk SI GaAs (with different crystal stoichiometries and with/without annealing) and the annealed LTMBE GaAs have been studied by a zero-bias TSC technique in both electrical and optical excitation modes. The main results are: 1) by eliminating the masking effect of the increasing I_{dark} at high temperatures, the ZBTSC(0) technique can reveal TSC peaks in the range of $81\text{K} < T < 380\text{K}$ and a peculiar spike feature at 235K; 2) the effectiveness of the technique for distinguishing crystal stoichiometry has been confirmed by using three bulk SI GaAs samples with different stoichiometries; 3) the driving force in the TSC current measurements under zero-bias comes from a non-equilibrium surface field as well as possibly from thermal gradient; 4) almost all the traps in the control SI GaAs samples can be found in the annealed LTMBE GaAs, but with higher trap densities in the latter; 5) the trap densities in annealed LTMBE GaAs are closely dependent on initial growth temperature.

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STUDY OF DEEP LEVELS IN LT-GaAs MATERIALS AND SI-GaAs WAFERS BY AN IMPROVED THERMOELECTRIC EFFECT SPECTROSCOPY

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ABSTRACT

We have developed a simpler and more reliable method of thermoelectric effect spectroscopy (TEES) by eliminating the second heater in the technique. We have applied this method to the deep level studies in semi-insulating (SI) GaAs epitaxial layers grown at a low temperature by molecular beam epitaxy (LT-GaAs) and SI-undoped GaAs, Cr-doped GaAs. We have found that the electrical contacts on front and back surfaces of the sample are more reliable for the TEES measurement than both contacts made on the same surface. In this contact arrangement, the temperature difference of about 1-2K between the back and front surfaces was enough to produce a clear and reliable TEES data, without the need for a second heater. The results obtained by TEES are consistent with the results obtained by photo-induced current transient spectroscopy (PICTS) and by thermally stimulated current (TSC) measurements. The TEES results clearly distinguish between the electron traps and the hole traps. We will discuss the results on the various semi-insulating GaAs samples and the advantages and limitations of the TEES technique.

I. INTRODUCTION

There exist several spectroscopic techniques for studying deep levels in semi-insulating (SI) III-V semiconductors. Thermally stimulated current (TSC)^[1] has a relatively small temperature range due to its large dark current when temperature is increased beyond a certain value (typically 250K). Photoinduced current transient spectroscopy (PICTS)^[2] is effective in determining the trap energy levels and the capture cross sections. These techniques, however, do not give a clear distinction between the electron and hole traps. Although it was claimed that under certain conditions, the type of a given trap could be determined by PICTS and/or TSC data, there was always some ambiguity and not all traps could be determined. Thermoelectric effect spectroscopy (TEES) was recently developed by Santic and Desnica^[3]. They added a second heater on the sample to create temperature gradient without any external applied bias. The thermal gradient induced enough electrical current with its sign corresponding to the type of dominant free carriers, and allowing the determination of the trap types.

II. IMPROVED METHOD OF THERMOELECTRIC EFFECT SPECTROSCOPY

The TEES arrangement is shown in Fig.1(a). We have found that a simple electrical connection between the front and back surfaces of the semi-insulating sample allowed the flow of thermoelectric current on the order of several picoamperes due to the temperature difference between the two surfaces on the order of 1K, as shown in Fig.1(b) for a 500 μ m-thick undoped SI-GaAs wafer. With this arrangement we could eliminate the need for a second heater and the possibility of an accidental reversal of temperature gradient that could occur when two heaters are used to create a small temperature difference in the sample. However,

when the sample was mounted with its edge on the sample mount, the temperature difference reversed its sign at about 120K, as Fig.1(c) shows. Therefore, the flat sample mount configuration was used. With our 500 μ m thick samples, the temperature difference between the front and back electrodes was measured to be 1.3K at 250K. The sample was first cooled down to the lowest temperature (16K) and then illuminated for a sufficient time (>10min.) Excitation light was provided by He-Ne laser (6.0mW). The contacts were made by soldering indium onto the sample without annealing. The TEES current was measured with Keithley Model 617 electrometer. The thermal scan was made at an average heating rate of about 0.35K/s from 60K to 420K. Below 60K, no current peaks were found.

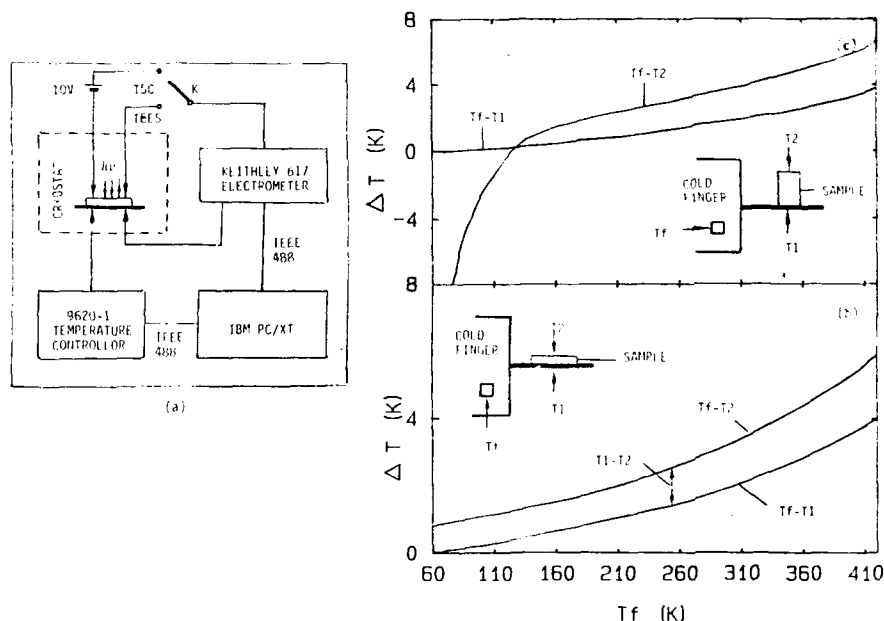


Fig.1. Schematic of (a) the experimental setup and the temperature difference in the sample mounted (b) on its surface and (c) on its edge. Note the crossover of T1 and T2 in (c), which could lead to a false identification of the trap type.

The temperature difference of about 1K (Ref.4) can be neglected in calculating the activation energy from the peak temperature positions. We may consider this as a thermally stimulated current with zero bias. For a single trap, the activation energy E_t can be obtained from Bube^[5], or roughly from:

$$E_t = kT_m \ln(T_m^4/\beta) \quad (1)$$

where T_m and β are the peak temperature and the rate of temperature increase, respectively. k is Boltzman constant. For $T_m > 100K$ and a small capture cross section $\sigma (< 10^{-15} \text{ cm}^2)$, the error is less than 0.05eV.

III. TEES ANALYSIS ON EPITAXIAL GaAs AND SEMI-INSULATING WAFERS

Figure 2(a) shows typical TEES spectra for the undoped SI-GaAs. The measurement circuit was connected in such a way that above the dark current, the peaks are hole traps, and the peaks below are electron traps (some exceptions will be discussed later). We have observed at least four hole traps and six electron traps in this undoped SI-GaAs sample. The

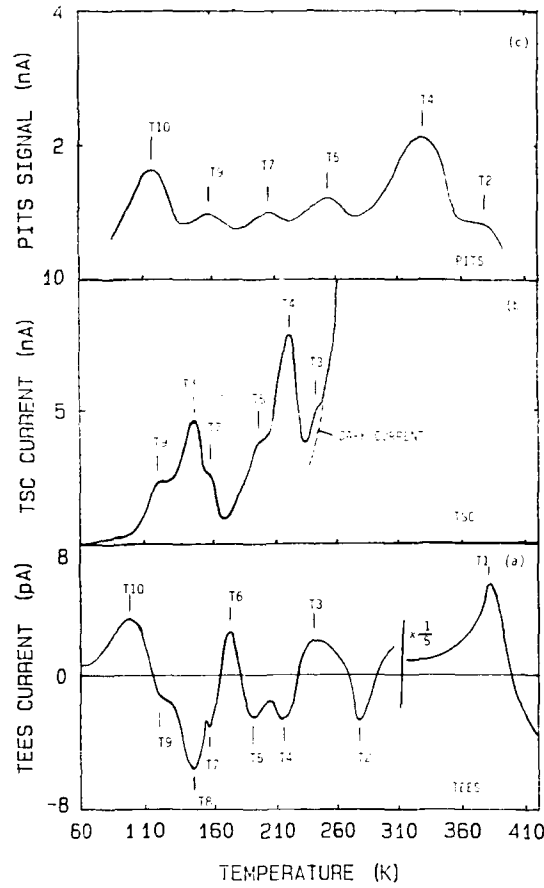


Fig.2. Measured (a) TEES, (b) TSC, and (c) PICTS signal vs temperature in the undoped SI-GaAs.

TSC and PICTS spectra of the sample are shown in Fig.2(b) and 2(c), and are consistent with the TEES data. More traps were observed by TEES due to its higher energy resolution than PICTS and TSC, and its capability to reach a higher temperature than TSC. The small dark current in TEES makes possible a higher temperature range scan than in the TSC. This is advantageous for studying deeper levels, like EL2. All observed traps and their possible identities are summarized in Table I.

Figure 3 shows the TEES spectra for the semi-insulating LT-GaAs epilayer, the undoped and Cr-doped SI-GaAs wafers. For comparison, we discuss the traps in the other two

samples in reference to the undoped sample. The up and down arrows indicate traps that are common with the undoped sample. The hole trap T3 and the electron traps T4 and T5 are common in all three samples. Fang et al. identified T4 as a hole trap, contrary to our results, and were unable to identify the type of T5, which is clearly an electron trap here. The electron trap T2 and the hole trap T10 are observed in both the undoped SI-GaAs materials and the LT-GaAs epilayers, but not in the Cr-doped SI-GaAs materials. The electron traps T7, T8, and T9 are commonly observed in the Cr-doped and undoped SI-GaAs bulk wafer, but not in the LT-GaAs epilayer. Also, there are some traps that are observed only in one sample: the hole trap T1 (0.82 eV) in the undoped SI-GaAs wafer; the hole trap C1 (0.55 eV) and electron traps C5 (0.30 eV), C9 (0.16 eV) only in the Cr-doped SI-GaAs wafer; and the electron traps LT1 (0.70 eV), LT6 (0.29 eV) and the hole traps LT6' (0.28 eV), LT7' (0.25 eV), and

TABLE I. Parameter of traps observed by TEES, TSC, and PITS in undoped SI-GaAs.

Label	TSC (eV)	PITS (eV)	TEES (eV)	Type	Identity	Reference
T1	0.82	H	HL10	6
T2	...	0.57	0.57	E	EL3	7
T3	0.47	...	0.46	H	Cu	8
T4	0.44	0.44	0.42	E	O or C	8
T5	0.37	0.37	0.38	E	EL6	9
T6	0.30	H	?	
T7	0.28	0.29	0.28	E		8
T8	0.26	...	0.25	E	V_{Ga}	10
T9	0.21	0.21	0.20	E	COMPLEX	8
T10	...	0.13	0.12	H		10

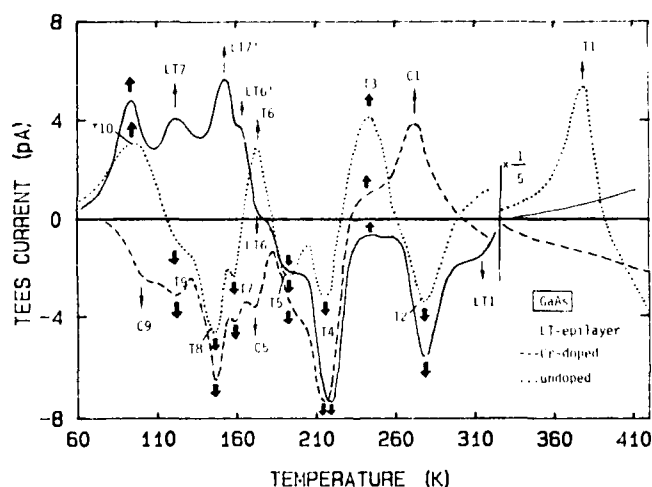


Fig. 3. Measured TEES spectra for different samples. (a) LT-GaAs, (b) undoped SI-GaAs, and (c) Cr-doped GaAs.

LT7 (0.20 eV) only in the LT-GaAs epilayer materials. The deep trap levels in the low-temperature GaAs epitaxial material are discussed in detail in our separate paper^[8]. When the cap-

ture cross section is large ($>10^{-14} \text{ cm}^2$), the activation energy estimated from Eq.(1) can be off the true value by as much as 0.1eV. The hole trap C1 is the case for which TEES and Eq.(1) give $E_t=0.55\text{eV}$ while the PICTS give $E_t=0.66\text{eV}$ and $\sigma=1 \times 10^{-14} \text{ cm}^2$. The electron trap C5 is very close to LT6 which is speculated to be M3^[8,11]. We are unaware of the literature source for the possible identity of C9.

Figure 4 shows the illumination time dependence of the TEES signal for the LT-GaAs sample. For most traps, the peak intensity clearly increases with the increasing illumination time. When a trap peak falls near the background level (i.e., zero current here) and is influenced by a nearby strong peak of opposite type, we could identify its type more clearly by change the illumination time, as demonstrated for LT3 in Fig.4. The illumination time dependence is not without problem, as seen for LT6. With increasing the illumination time, LT6 progresses like a hole trap. However, a more careful study of this peak in various LT-GaAs samples made us identify this peak as an electron trap (see Ref.8 for details). The progression

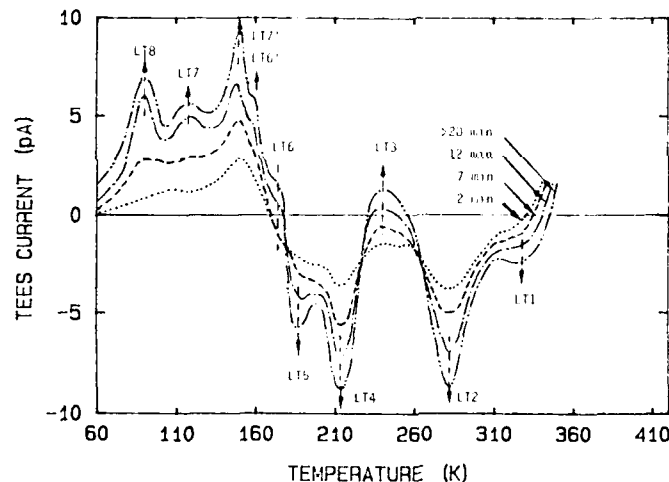


Fig.4. Illumination time dependence of TEES signal for LT-GaAs.

of LT6 with illumination appears to be dominated by the nearby hole traps LT6' and LT7' rather than by its own type. This aspect has to be considered carefully in determining the types of very small peaks.

The TEES current is in the order of picoamperes as we showed above, it could be affected by some other factors. Two major factors are, for example, the off-set of the Keithley 617 electrometer and the built-in surface field due to the two contacts. However, an off-set of about 0.1-0.3mV can provide the current in only one direction (either positive or negative), it can be treated as a dark current. In order to see the influence of the built-in surface field, we mounted the sample on its edge as shown in Fig.1(c), and made the contacts at the same height from the holder on two surfaces so that there was no temperature difference between two contacts. Other measurement conditions were kept the same. The results showed that the current was very small, and also the polarity of the current was disappeared, indicating that the influence from surface field is small compared with the TEES current.

IV. SUMMARY

In summary, an improved thermoelectric effect spectroscopy technique has been presented with improved results on the LT-GaAs epitaxial materials. In comparison, we have discussed the results in undoped SI-GaAs and Cr-doped SI-GaAs wafers. At least four hole traps and six electron traps were found in undoped SI-GaAs. The illumination time dependence of the TEES spectra is useful for a more clear identification of some small peaks. This TEES method is useful for deep level studies in other semi-insulating III-V materials due to its high sensitivity and reliable and a larger temperature range of measurement.

ACKNOWLEDGMENT

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ELECTRON PARAMAGNETIC RESONANCE STUDY OF LOW TEMPERATURE MOLECULAR BEAM
EPITAXY GROWN GaAs and InP LAYERS

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ABSTRACT

The native defects in LTMBE III-V layers have been studied by the electron paramagnetic resonance (EPR) technique for three different systems: GaAs on GaAs, GaAs on Si and InP on InP. The GaAs layers are characterised by high concentrations of ionized arsenic antisite defects (10^{19} cm^{-3}), with properties similar to those of the native As_{Ga} in amorphous GaAs. Their variation with the growth temperature, layer thickness and thermal annealings has been assessed. The results are independent on the nature of the substrate, GaAs or Si. In spite of a 1% phosphorous excess no phosphorous antisites could be detected in the as-grown, undoped or Be doped InP layers.

1. INTRODUCTION:

Semi-insulating undoped GaAs layers grown by the low temperature molecular beam epitaxy on GaAs substrates have been shown to have interesting technological applications, ranging from buffer layers in GaAs based MESFET, MODFET and HEMT structures to the application in ultrafast detectors due to small minority carrier lifetimes [1]. The electrical [2,3] and optical [4,5] properties of these layers are quite distinct from those obtained by "classical" high temperature MBE layers grown in the 600°C temperature range. Whereas these layers are characterised by low native defect concentrations ($\approx 10^{14} \text{ cm}^{-3}$), the LTMBE layers contain native defects in the 10^{19} cm^{-3} concentration range. Among them only an arsenic antisite related defect has been identified [6,7], as in the case of meltgrown GaAs, where the semi-insulating properties are equally related to an arsenic antisite related defect, EL2 [8].

LTMBE GaAs layers with these particular properties can only be grown in a limited temperature range at 200°C, as for lower temperatures polycrystalline or amorphous layers are formed and for higher temperatures the defect concentration diminishes rapidly. The as-grown layers are highly instable to thermal annealing and in fact due to their low electrical resistivity would not be of interest in the above cited applications. It is only in the annealed state, which is often implicitly obtained by active layer overgrowth in the 600°C temperature range, that the layers are of high electrical resistivity ($>10^6 \text{ cm}$)

For an optimisation of growth conditions and post growth treatments of these layers an analysis of the native point defects is of interest. Thus we have undertaken an electron spin resonance (EPR) study of the defects in LTMBE GaAs layers grown on GaAs substrates as a function of growth temperature, sample thickness as well as furnace annealing. We have further extended these studies to LTMBE layers grown on silicon substrates, where their usefulness for the fabrication of high power field effect transistors has been demonstrated recently [9].

The intrinsic origin of the native defects indicates a possible extension of the LTMBE growth technique to other III-V compounds. In particular the InP system suffers from the inavailability of highly

resistive, thermally stable, epitaxial layers and thus is a good candidate for such a study. We report first EPR results on LTMBE InP layers grown by gas source MBE at 200°C.

2. EXPERIMENTAL

The defects in three types of layers, GaAs on GaAs, GaAs on Si and InP on InP, have been analysed by electron paramagnetic resonance. We used an X-band EPR spectrometer allowing in situ optical excitation in the 0.8 to 2.5 μm spectral range and sample temperatures between 4K and 20K. Some of the samples have equally been analyzed by optical absorption spectroscopy. Typical sample dimensions are 4x8 mm². Care has been taken to separate the defects in the thin epitaxial layer from those in the $\approx 500\mu\text{m}$ thick substrate, which in the case of the study of arsenic antisite defects in GaAs on GaAs samples can easily give rise to confusion.

The GaAs layers were grown in a Varian 360 system under normal, As-stabilized conditions, at a growth rate of 0.8 μm per hour on semi-insulating GaAs substrates. The substrate temperature was varied between 200 and 300°C and layers with thicknesses between 2 and 15 μm were grown. The 5 μm thick GaAs layers on Si were grown under similar conditions at 200°C. The samples were furnace annealed for 15 min in flowing argon under face to face protection, at successive temperatures of 300, 400 and 500°C.

The InP layers were grown by Gas Source MBE with a phosphine precursor at a temperature of 200°C under phosphorous rich conditions on semi-insulating Fe doped substrates; more details can be found elsewhere [10]. Typical layer thickness is 2 to 10 μm . Both undoped and Be doped layers have been studied. A secondary ion mass spectroscopy analysis showed these layers to be heavily contaminated with H in the as grown state.

3. RESULTS

3.1 GaAs on GaAs

Figure 1A shows a typical thermal equilibrium EPR spectrum of a 5 μm thick layer grown at 200°C.

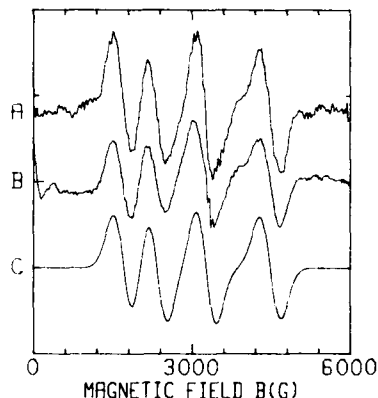


Fig. 1: EPR spectrum of GaAs/GaAs (A), GaAs/Si (B) and simulated spectrum (C), ($A=866 \times 10^{-4} \text{ cm}^{-1}$)

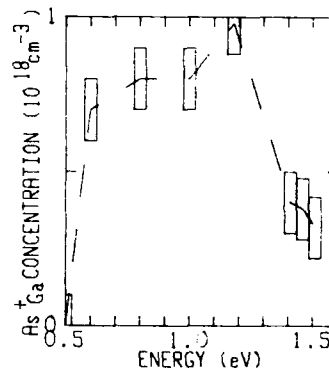


Fig. 2: Photoexcitation Spectrum of the As_{Ga} defect

It consists of an isotropic four line spectrum, already previously attributed to an arsenic antisite defect

[6,7,11,12]. The spectrum is characterised by its g-factor and its hyperfine coupling constant A, which are derived with the Breit-Rabi formula:

$$g=2.04\pm0.01$$

$$A=(866\pm10)\times 10^{-4} \text{ cm}^{-1}$$

The hyperfine coupling constant is significantly different from the one of the EL2 related antisite defect, whose value is $(890\pm10)\times 10^{-4} \text{ cm}^{-1}$ [13]; its value changes with the thermal annealing as we will see below. Optical absorption on these layers show a strong absorption band in the 1.05eV to 1.35eV range with absorption coefficients of $\approx 10^3 \text{ cm}^{-1}$, which in analogy to the intracenter transition of the neutral EL2 defect have been attributed to the neutral AsGa^0 defect. Assuming similar oscillator strengths for the two defects, an AsGa^0 concentration of $\approx 10^{19} \text{ cm}^{-3}$ has been deduced from this absorption coefficient [4,5].

By comparison with a spin standard sample we determined the ionised AsGa^+ concentration; values between 2 and $9\times 10^{18} \text{ cm}^{-3}$ are found for the as-grown (200°C) samples.

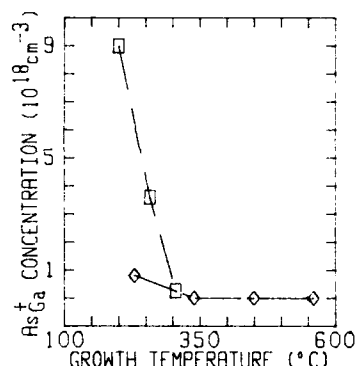


Fig.3: $[\text{AsGa}^+]$ as a function of growth temperature for one undoped (□) and one Si (◇) doped sample

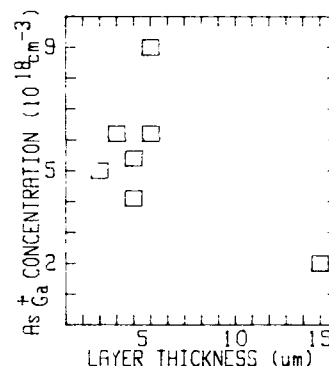


Fig.4: $[\text{AsGa}^+]$ as function of layer thickness

Low temperature photoexcitation with below bandgap light leads to a metastable change in the AsGa^+ concentration. In all samples only an optically induced increase in the AsGa^+ concentration is observed with no indication of EL2 like photoquenching. Its spectral dependance, determined by the saturation values for each photon energy, is given in fig.2. The onset of $E=0.6\text{eV}$ is shifted by $\approx 0.2\text{eV}$ to lower energies as compared to the corresponding photoionisation spectrum of EL2. The simultaneous increase of the AsGa^+ and decrease of the AsGa^0 concentration demonstrate, that the effect of excitation is a transfer of electrons from the neutral AsGa^0 centers to other non identified electron traps and not photoquenching of the AsGa defect, as might have been deduced from the optical absorption results alone.

Figure 3 shows the dependance of the equilibrium AsGa^+ concentration on the growth temperature for two series of $5\mu\text{m}$ thick layers, one undoped (□), the other (◇) Si doped. We see, that a change from 200°C to 250°C leads already to a reduction in AsGa^+ by a factor of ≈ 3 and a change to 300°C to a further reduction by a factor of ≈ 10 .

It has been shown previously, that under the growth conditions used here for thicknesses above a critical thickness of $3\mu\text{m}$ pyramidal defects containing polycrystalline cores are formed [14] and it has been speculated, that the AsGa defects are related to these extended defects. In this context we have studied three layers of $2, 3, 4\mu\text{m}$ thickness (fig.4) and determined their respective AsGa^+ concentrations: we find $5.0, 6.3$ and $5.5 \times 10^{18} \text{ cm}^{-3}$, thus a thickness independent concentration. However different growth conditions at a fixed temperature (200°C) and layer thickness can lead to a variation of AsGa^+ by a factor of 3 (fig.4).

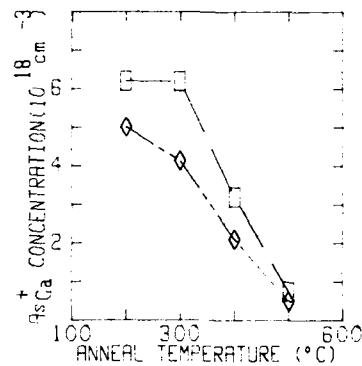


Fig.5: $[\text{AsGa}^+]$ as a function of thermal annealing
(\square) GaAs/Si, (\circ) GaAs/GaAs

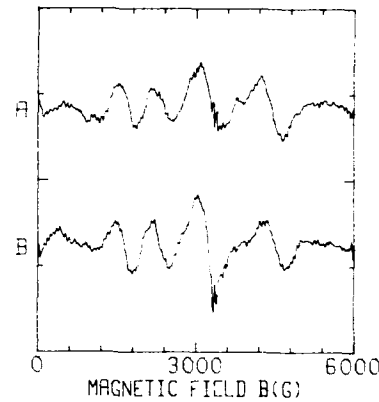


Fig.6: thermally annealed part of the EPR spectrum (A) 400°C , (B) 500°C

Previous results have shown a thermal instability of the 200°C grown layers in the 300 to 500°C temperature range [2,4,6,11], which must be related to the generation or annealing of the native defects. In optical absorption measurements [4] a decrease in the neutral AsGa^0 concentration from $3 \times 10^{19} \text{ cm}^{-3}$ to $3 \times 10^{18} \text{ cm}^{-3}$ has been found after annealing at 500°C . We have measured in different samples the corresponding change in the ionised AsGa^+ concentration in order to clarify, whether the total arsenic anneals out at this low temperature or whether the annealing leads just to an increase in the compensation ratio. The results for a $2\mu\text{m}$ thick sample, given in fig.5 (\circ), confirm, that the AsGa defect is already unstable at 300°C .

The thermal annealing does equally change the hyperfine interaction constant of the AsGa^+ defect. After a 400°C annealing the A value of the remaining AsGa changes from $866 \times 10^{-4} \text{ cm}^{-1}$ to $890 \times 10^{-4} \text{ cm}^{-1}$; analyzing the difference spectra - $300^\circ\text{C} - 400^\circ\text{C}$ - we find, that the AsGa^+ defect, which anneals out at 400°C has even a still smaller value of $A = 833 \times 10^{-4} \text{ cm}^{-1}$. The total EPR spectrum before the anneal can be simulated by the superposition of those of two distinct AsGa defects with A-values of 833 and $890 \times 10^{-4} \text{ cm}^{-1}$ and comparable concentrations, but different thermal stability, which give rise to an effective A value of $866 \times 10^{-4} \text{ cm}^{-1}$ (fig.6). Further annealing studies and simulations are under way to confirm this point.

The LTMBE GaAs layers deposited on intrinsic Si substrates showed in all aspects identical defect behaviour as those deposited on the GaAs substrates: once again the As_{Ga} defect is the dominant native defect, with the same EPR parameters g,A inspite of the important lattice mismatch (fig. 1B).; the ionized As_{Ga}^+ concentration of $6 \times 10^{18} \text{ cm}^{-3}$ is also typical for $5 \mu\text{m}$ thick layers grown on GaAs substrates. The annealing of As_{Ga}^+ proceeds equally in the 300 to 500°C temperature range with final concentrations of some 10^{17} cm^{-3} (fig. 5). The difference spectra of the 300/400°C and 400-500°C annealing steps can again be interpreted by (fig.6) the presence of two different As_{Ga} defects.

3.3 InP on InP : Fe

The successful growth of monocrystalline LTMBE InP layers at temperatures of 200°C has recently been demonstrated [10]. These layers are characterized by phosphorous excess of $\approx 1\%$, increased lattice constants as compared to bulk grown InP but also by high hydrogen contamination due to the phosphine precursor. Both undoped and Be doped (attempted doping concentration of $\approx 10^{18} \text{ cm}^{-3}$) non annealed layers have been studied.

The EPR analysis of these layers is complicated by the strong Fe^{3+} background signal coming from the InP substrate. No paramagnetic defect could be detected in those layers, neither at thermal equilibrium nor under photoexcitation. The coupling of the EPR cavity indicates, that even at 4K the undoped and Be doped InP layers are still of low resistivity and thus the Fermilevel pinned by the shallow donors. Under such conditions the phosphorous antisite is neutral and diamagnetic. Its EPR observation is only expected after electrical activation of the Be dopants, the conditions for which are still studied

4. DISCUSSION

Our EPR results on the LTMBE GaAs layers demonstrate in agreement with previous results, that arsenic antisite related defects are the dominant native defects in these layers with concentrations up to 10^{19} cm^{-3} . These antisite defects are different from EL2, as deduced from the smaller hyperfine interaction constant, the energy shift of the onset of the photoionization spectrum of As_{Ga}^0 , the absence of photoquenching as well as the lower thermal stability. Our calculations based on [16] show, that the change in the hyperfine interaction constant is not due to the difference in the lattice parameters of LTMBE and bulk grown GaAs. The results are given in figure 7, a change in the lattice

	$A \times 10^{-4} \text{ cm}^{-1}$	Quench
EL2	890	yes
a-GaAs	866	no
LTMBE	866	no
e-n type	680	no
e- n type	867	no
e- p type	890	no
e- si	890	no

Table I

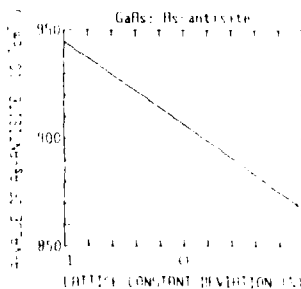


Fig7 Variation of A with the lattice constant

parameters by 0.1% is expected to change the A value by only $5 \times 10^{-4} \text{ cm}^{-1}$. Thus the lower A value has to be attributed to a change in the defect configuration and thus the defect to a different As_{Ga} complex. As_{Ga} defects with different A values have been observed before; they occur as native defects in Czochralski and Bridgman grown GaAs, amorphous MBE grown GaAs and can be formed by electron irradiation. Their respective hyperfine interaction constants, which are fingerprints for specific defect configurations, are given in table 1: we see, that As_{Ga} defects with the same A value and at comparable concentrations have been detected as native defects in amorphous MBE grown GaAs [16]; they can also be formed by electron irradiation in n-type GaAs [17]. This could be an indication for initial mixed amorphous/ crystalline phases in the growth process, which indeed been observed before in MBE growth of GaAs at 200°C and found to depend strongly on the III to V flux ratio [18].

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Optically Detected Magnetic Resonance of Arsenic Antisites in GaAs MBE Layers Grown at Low Temperatures

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ABSTRACT

Observation of Arsenic antisites (As_{Ga}) in GaAs layers grown by molecular beam epitaxy (MBE) at low substrate temperatures ($\sim 200^\circ\text{C}$) is reported, using electron paramagnetic resonance (EPR), magnetic circular dichroism in absorption (MCDA), and MCDA tagged by optically detected magnetic resonance (MCDA-ODMR). This experiment confirms that there is a MCD absorption band directly associated with As_{Ga} in the GaAs layers. The As_{Ga} concentration in the GaAs layers is found to decrease by about one order of magnitude after annealing at 600°C for two minutes.

INTRODUCTION

Thin epitaxial GaAs layers grown by molecular beam epitaxy (MBE) at unusually low temperatures (LT) between $200 - 300^\circ\text{C}$, as opposed to the regular growth temperatures of $550 - 600^\circ\text{C}$ for GaAs, are of current interest in view of their technological importance as insulating buffer layers in GaAs devices and integrated circuits,^{1,2} as well as many unusual physical properties such as the recently-reported superconductivity.³ Despite the low growth temperatures, LT GaAs layers remain crystalline up to a limited epitaxial thickness.⁴ A high concentration of compensating deep-level defects is introduced during growth, being responsible for the desirable high resistivity of the material. Using electron paramagnetic resonance (EPR), the dominating point defects of the material have been identified as arsenic antisites (As_{Ga} , an arsenic atom occupies a gallium site) with concentration as high as $\sim 10^{19}\text{ cm}^{-3}$ in as-grown layers.⁵ In this paper, we would like to report the first direct optical detection of As_{Ga} in such layers using magnetic circular dichroism in absorption (MCDA) and MCDA tagged by optically detected magnetic resonance (MCDA-ODMR).⁶

MCDA-ODMR is a well-established technique to probe chemical signatures of As_{Ga} in GaAs bulk materials, such as the well-known EL2 center.⁷ Not only is the sensitivity of the technique often higher than that of conventional EPR, but also it links the EPR signature of a paramagnetic defect under investigation with the MCD of an absorption band associated with that defect.

EXPERIMENTAL CONDITIONS

The measurements were done on $3\text{-}\mu\text{m}$ MBE-grown LT GaAs single layer on (100) semi-insulating GaAs substrates. The layer was grown around 200°C in the MBE machine of US Army ETD Laboratory, and it was not annealed above the growth temperature in the machine. For a preliminary annealing study, a standard rapid thermal annealer was used to anneal samples at 600°C for 30 seconds or 120 seconds. The as-

grown layer quality was reasonable, as shown in Fig. 1 by double-crystal x-ray diffraction of the LT GaAs layer and the substrate. The peak for the LT GaAs layer is fairly narrow, even though it is not as narrow as that for the substrate, indicating that the layer is predominantly crystalline with some degree of imperfection, such as dislocations; however, the possibility has not been ruled out that there could be a thin amorphous layer on top of the epitaxial due to a limited epitaxial thickness.⁴ From the x-ray data, the lattice mismatch is estimated to be about 0.07%.

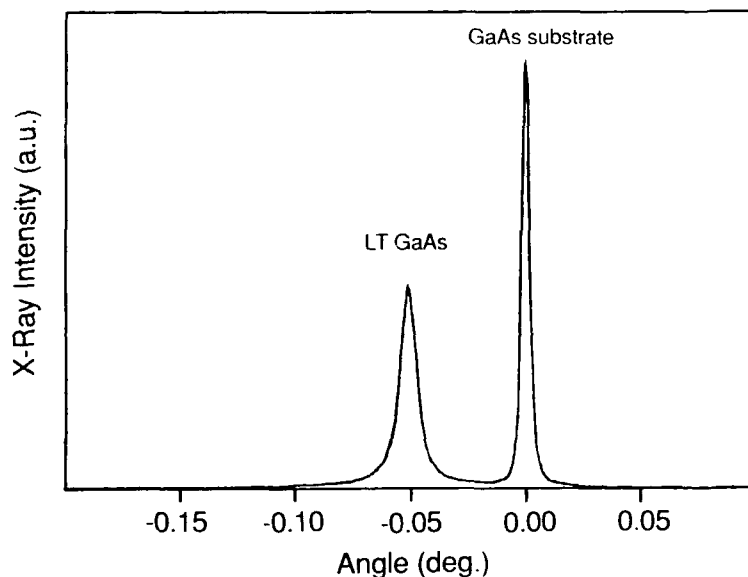


Fig. 1. Double-crystal x-ray diffraction from the (400) planes of as-grown LT GaAs on a SI GaAs substrate.

To obtain reasonable signal to noise ratios, a stack of four 4x20 mm² single-layered pieces (320 mm² of total layer area) was used for EPR characterization, and a single 1x2 mm² piece (2 mm² of total layer area) for the MCDA and MCDA-ODMR measurements. For all practical purposes, there were no observable EPR and MCDA-ODMR signals from the substrate material, which is highly desirable for this study. A Bruker ESP300 X-band EPR spectrometer was employed for EPR measurements. The MCDA and MCDA-ODMR experiments were performed at pumped-liquid-He temperatures ($T \sim 1.5\text{K}$) in an optical cryostat with a 3-Tesla superconducting magnet, at Sherman Fairchild Laboratory of Lehigh University. A sample was mounted, with magnetic field parallel to the [100] direction of the sample, in a Q-band ($\sim 35\text{ GHz}$) TE_{011} microwave cavity with abundant optical access. The light source was a 600-W tungsten halogen lamp dispersed by a quarter-meter monochromator. Alternating right and left circularly polarized components of the light were generated by an infrared linear polarizer in conjunction with a quartz stress modulator operating at 50.3 kHz. The transmitted light propagating along the static magnetic field direction was monitored by a fast-response Ge detector, the difference between the right and left components being obtained by lock-in detection at 50.3 kHz. The MCDA intensity is given by the ratio of the lock-in detected signal to the total transmitted right and left components. For the MCDA-ODMR exper-

iment one measures changes in MCDA induced by EPR transitions of a paramagnetic state of a defect center. The details of the MCDA and MCDA-ODMR apparatus are described elsewhere.⁸

RESULTS AND DISCUSSIONS

The presence of As_{Ga} defects in the as-grown LT layer was demonstrated by EPR, which is shown in Fig. 2. The concentration of As_{Ga} is estimated to be in the order of $10^{19}cm^{-3}$ which is consistent with the previously-reported value.⁵ An exact spin Hamiltonian analysis shows that the EPR spectrum can be reasonably matched, but not exactly, using the g-value, $g = 2.04(1)$, and a hyperfine constant, $A = 2665(30)$ MHz for the EL2 center.⁹ The EPR signal completely disappeared after the layer was removed from the substrate, establishing that the EPR signal originated entirely from the LT layer.

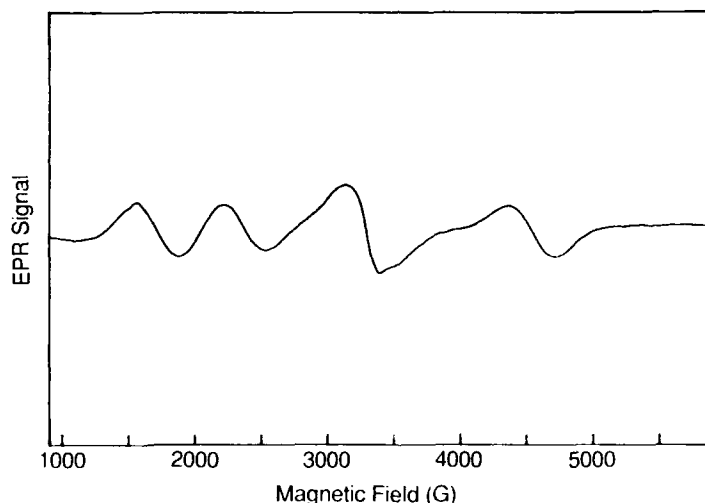


Fig. 2. X-band EPR spectrum of as-grown LT GaAs on SI GaAs substrate at $T = 10$ K, with magnetic field parallel to $[100]$.

The MCDA spectrum of the as-grown LT GaAs sample is shown in Fig. 3 (a); the MCDA signal became too weak to measure at higher photon energy because of much stronger absorption. In the detected energy range, the MCDA spectrum appears to be similar to that of the EL2 center.^{7,9} The corresponding MCDA-ODMR spectrum is shown in Fig. 4 (a) when the MCDA photon energy of $0.93eV$ ($\lambda = 1330$ nm) was selected. The MCDA-ODMR spectrum is corrected for the magnetic field dependence of MCDA. Clearly, a strong signal due to As_{Ga} is observed. The four arsenic hyperfine lines are only partially resolved because of broad line width, most likely reflecting the fact that some part of the LT film is not strictly crystalline, i.e., there is a distribution of different As_{Ga} defects due to disorder in that part of the layer. It was impossible to match exactly the four resonance positions using the exact spin Hamiltonian analysis for As_{Ga} . Nonetheless, this observation identifies that the MCDA band is directly associated with As_{Ga} .

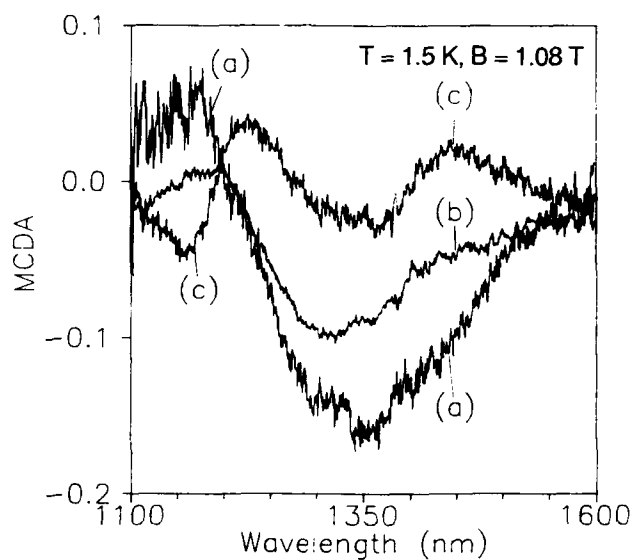


Fig. 3. MCDA spectra of as-grown LT GaAs on a SI GaAs substrate: (a) $3\ \mu\text{m}$ LT layer, (b) after etch ($\leq 4\ \mu\text{m}$ LT layer remaining), and (c) after mechanical polish to completely remove the LT layer.

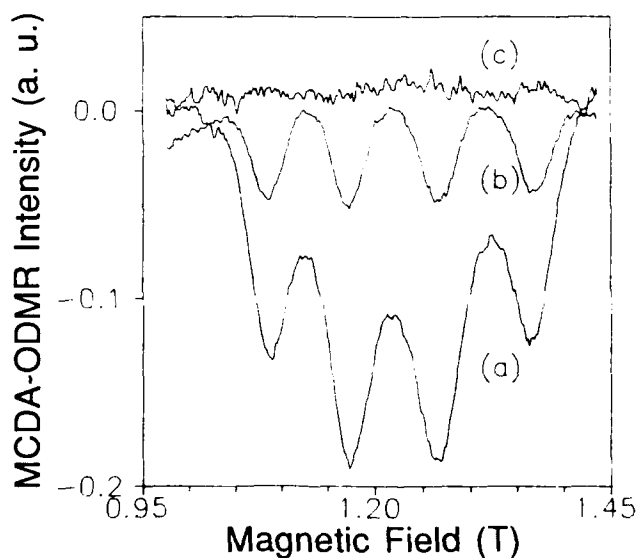


Fig. 4. O-band MCDA-ODMR spectra of as-grown LT GaAs on a SI GaAs substrate at $T = 1.5\text{ K}$, with magnetic field parallel to $[100]$: (a) $3\ \mu\text{m}$ LT layer, (b) after etch ($\leq 4\ \mu\text{m}$ LT layer remaining), and (c) after mechanical polish to completely remove the LT layer.

After etching the LT layer, due to an accidental non-uniform etch, there was less than $1\mu\text{m}$ LT GaAs layer remaining on the substrate. The corresponding MCDA spectrum, which is shown in Fig. 3 (b), is still about the same as that before etch, even though its intensity is weaker than before, as expected. The MCDA-ODMR spectrum of the remaining layer is shown in Fig. 4 (b), which is, however, quite different from that before etch. Clearly, the intensity is less than one third of that before etch. Most dramatically, the four-line hyperfine structure is completely resolved and spectroscopically different from before. The four resonance positions can now be fit to an arsenic antisite spin Hamiltonian almost exactly, yielding the g-value, $g=2.037(1)$, and the hyperfine constant, $A = 2691(2)$ MHz. This observation strongly suggests that there is only one kind of As_{Ga} in the remaining LT film which is most likely crystalline.⁴ The remaining film was completely removed by mechanical polishing, and then the MCDA-ODMR signal vanished, as shown in Fig. 4 (c), suggesting that the substrate material has no contribution to the MCDA-ODMR of As_{Ga} . The corresponding MCDA spectrum of the substrate without any LT layer is shown in Fig. 3 (c). Collectively, our observations support the notion that there is only one kind of As_{Ga} in epitaxial LT GaAs layers, and there is a distribution of different As_{Ga} defects in the poor epitaxial region.

One of the important questions about these arsenic antisites is whether they are associated with the much-studied EL2 center or not. In order to answer this question, high-resolution optically detected electron-nuclear double resonance (ODENDOR)¹⁰ was attempted on these antisites in the LT GaAs layers, crystalline or crystalline/amorphous mixture. Unfortunately, no ODENDOR signal has been observed in our samples. The search still continues. In a previously-reported study, Kaminska et al.¹¹ have demonstrated that the As_{Ga} center in LT GaAs is partially optically quenchable, as observed for the EL2 center. However, the spectral response of quenching efficiency differs substantially from that of EL2.

In an earlier EPR study,⁵ Kaminska et al. have shown that EPR was not sensitive enough to observe As_{Ga} in LT (200°C) GaAs layers annealed at 600°C ; therefore, the antisite concentration after annealing could not be obtained. Annealing LT GaAs at 600°C after growth is an important processing step to improve the electrical properties of LT GaAs for application in device structures. From our preliminary annealing study, shown in Fig 5, we found that MCDA-ODMR of As_{Ga} is still detectable in our samples annealed at 600°C for two minutes. From the intensity changes in MCDA, the As_{Ga} concentration is estimated to have decreased by about one order of magnitude upon annealing at 600°C for two minutes. A complete annealing study is under way.

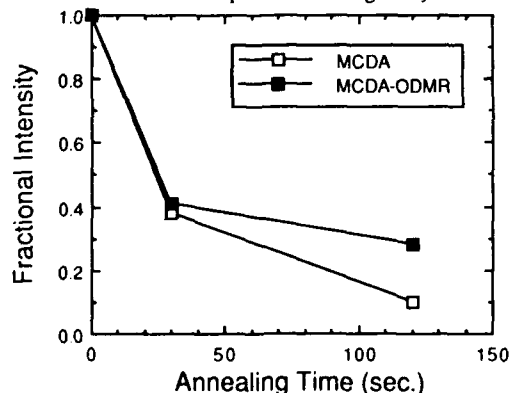


Fig. 5. Fractional intensity of MCDA ($\lambda \sim 1330$ nm) and MCDA-ODMR of As_{Ga} in LT GaAs annealed at 600°C as a function of annealing time.

CONCLUSIONS

In summary, we have observed MCDA and MCDA-ODMR of As_{Ga} in as-grown LT GaAs layers. We have demonstrated that the MCDA-ODMR technique is very suitable to study LT GaAs thin layers. A single As_{Ga} center is found in good epitaxial LT thin layers. A distribution of different As_{Ga} centers has been observed in low-quality LT layers. Perhaps most importantly, we have demonstrated that there is an EL2-like MCDA band directly associated with As_{Ga} in LT GaAs. Since MCDA is closely related to absorption, the strong infrared absorption band from 0.8 to 1.4 eV of LT GaAs originates, at least in part, from As_{Ga} . The As_{Ga} concentration in these layers dropped by one order of magnitude after annealing at 600°C for two minutes.

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CATHODOLUMINESCENCE AND PHOTOLUMINESCENCE SPECTROSCOPY STUDY OF LOW TEMPERATURE MOLECULAR BEAM EPITAXY GaAs

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ABSTRACT

We report a cathodoluminescence (CL) and photoluminescence (PL) study of molecular beam epitaxy grown GaAs at low substrate temperatures (LT GaAs), and semi-insulating LEC GaAs. The *as grown* LT GaAs material shows intense deep level emissions which can be associated with an excess concentration of Arsenic. These emissions subside with annealing for a few minutes at temperatures above 450 °C. CL measurements clearly show an extremely reduced concentration of traps in the post-growth 600 °C annealed material. These results account for a diminished role of electronic point defects in controlling the insulative behavior of LT GaAs and strongly support the "buried" Schottky barrier model.

INTRODUCTION

Recently, a new kind of GaAs, named low temperature (LT) GaAs,¹ was shown to have extremely high resistivity, high crystalline quality, and high carrier mobility. All these properties make LT GaAs an excellent material for device applications.^{2,3} The origin of the insulative behavior in LT GaAs is still a subject of controversy.⁴⁻⁶ Two dissimilar mechanisms of insulation have been proposed. One model assumes dopant compensation by point defects in the semiconductor,^{4,5} and it is similar to the model proposed for explaining insulation in semi-insulating (SI) *melt-grown* GaAs. A second model suggests that As precipitates act as buried Schottky interfaces whose overlapping depletion regions render the material semi-insulating.⁶

A brief summary of the properties of LT GaAs follows. During MBE growth of GaAs at low substrate temperatures, in the range 200-250 °C, large amounts of Arsenic are incorporated within the epilayer.² This excess As, of the order of 1-2% or mid 10^{20} cm^{-3} ,² was shown to be mostly in the form of As_{Ga} antisite defects.^{2,7,8} X-ray rocking curves indicate a lattice expansion of the LT GaAs of about 0.1%.² This expansion may be caused by the excess As arranged as interstitials, and was shown to scale with the amount of excess As.^{2,7} These epilayers are conductive, and the temperature dependence of the conductivity follows the $1/4^{\text{th}}$ power law characteristic of hopping conduction.^{5,9} Raising the substrate temperature to normal growth temperatures, typically 600 °C, results in the excess arsenic forming clusters, called As precipitates,^{8,10,11} and in a decrease of the lattice constant to values closer to the characteristic value of GaAs.^{2,7} Transmission electron microscopy (TEM) studies of LT GaAs grown at 250 °C and annealed at 600 °C indicate a density of As precipitates of the order of 10^{17} cm^{-3} , with an average diameter in the range 3 - 10 nm and average spacing of about 20 nm.^{8,10,11}

Here we report an optical emission study of the kinetics of formation of Arsenic precipitates and associated deep level defects in LT MBE GaAs. We also carried out measurements on semi-insulating (SI) LEC GaAs. Our measurements clearly indicate a dramatically reduced concentration of traps in the post-growth annealed LT GaAs. These results account for a diminished role of electronic point defects in controlling the insulative behavior of LT GaAs and strongly support the "buried" Schottky barrier model,⁶ which involves ultra fast recombination of carriers at surfaces of embedded Arsenic clusters formed during the annealing processing of the LT GaAs.

EXPERIMENTAL PROCEDURES

Arsenic cap		
LTBL	1 μm	
GaAs temperature transition region		
	0.25 μm	
$\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$	500 Å	
n-GaAs	$1 \times 10^{18} \text{ cm}^{-3}$	0.5 μm
n ⁺ GaAs Substrate		

Figure 1. Sample cross section

The films used in this work were grown in Varian GEN II MBE systems on two inch diameter substrates. A detail explanation of the growth procedures appears elsewhere.¹³ Several specimens, which mostly differ in post-growth processing, were grown: standard MBE GaAs grown at 600 °C, and LT MBE GaAs grown at 250 °C, with and without post-growth annealing at 600 °C under As overpressure. Figure 1 shows a typical cross-section of the specimens multiple layer structure used in this work. Following MBE growth the specimens surfaces were "capped" *in situ* with several hundred angstroms of As as protection against ambient contamination.¹⁴ These caps are thermally desorbed in UHV to provide clean ordered GaAs surfaces, as determined by LEED and Auger spectroscopy measurements.^{14,15} Experiments were also performed on SI melt grown GaAs (source: Cominco Electronic Materials). Experimental procedures for the CLS, PLS, and LEED measurements appear elsewhere.¹⁴

RESULTS AND DISCUSSION

Low energy cathodoluminescence spectroscopy has been shown to be an extremely sensitive technique for studying optical emission properties of III-V semiconductors at both the surface and near surface region of the material.^{12,14} Some of the advantages of electron excitation over photon excitation derive from the gaussian shape of the energy loss profile and the control of the excitation depth provide by CL.¹⁶ This depth becomes smaller with decreasing electron beam energy, rendering the corresponding luminescence spectra more surface sensitive. In order to illustrate these points, in figure 2 we depict room temperature PL and CL spectra of 580 °C "decapped" MBE GaAs (100), and of LEC GaAs. The desorption of the As cap and subsequent sample heating up to 580 °C was shown to produce high quality surfaces, with enhanced near band gap (NKG) luminescence intensity and reduced surface deep level emissions.^{14,15} The depth resolved CL spectra show very small emission intensity from deep levels. However, PL spectra obtained with 1.96 eV photoexcitation show much more intense deep level emissions than the surface sensitive CL spectra. The spectral shape and energies of these deep level emissions are similar to that of the LEC GaAs substrate, as shown by PL and CL measurements

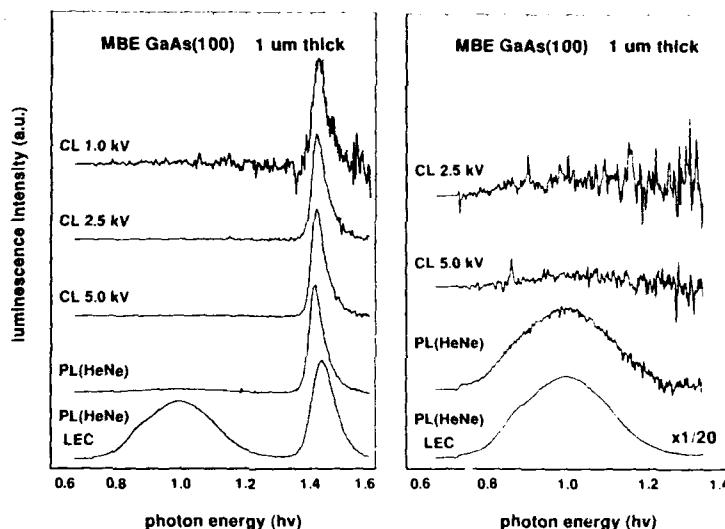


Figure 2. CL and PL spectra of clean ordered MBE GaAs and of LEC GaAs. The figure on the right side shows in detail the deep level CL spectra.

performed on GaAs substrates. These results indicate that, in this case, the source of these deep level emissions lies in the GaAs substrate. On the other hand, the much better bulk semiconductor quality of MBE GaAs is shown in the orders of magnitude reduced deep level emission intensity of the CL spectra. Figure 2 clearly demonstrates the advantages of controlling the depth of carrier excitation when studying localized semiconductor deep level states and assessing the spatial source of the emissions.

Figure 3(a) depicts RT CL and PL spectra of *as-grown* LT GaAs annealed for 10 minutes at 400 °C. The As cap is mostly desorbed at this temperature. LEED patterns show a 2x4 reconstruction with a high background intensity which is indicative of residual surface disorder.¹⁵ Annealing at about 425 °C improves the surface quality. All the spectra show relatively large emission intensity from deep levels, which indicates a large amount of defects present in this material. This high trap density and the specimen layer structure, which includes a 50 nm $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ barrier, obstructs carrier diffusion into the GaAs substrate, thereby diminishing the contribution of the substrate to the PL spectra. This observation of deep levels in pre-annealed LT GaAs agrees with previous observations by other techniques carried out on *as-grown* materials.^{7,8} The dominant emission at around 1 eV can be assigned to a transition involving the electronic trap EL2 and the VB. This band assignment is based on the identification of EL2 as the deep level responsible for the 1 eV infrared absorption observed in SI GaAs wafers.¹⁷ The shoulder at about 0.85 eV, whose relative intensity increases towards the surface, can be associated with emission from surface states.¹⁴

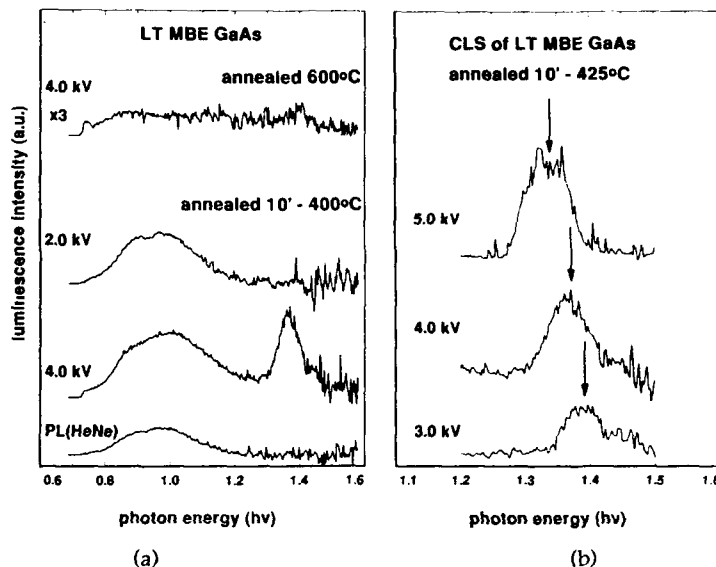


Figure 3(a). CL and PL spectra of as-grown LT GaAs annealed for 10 minutes at 400 °C. The figure also shows a spectrum of LT GaAs annealed at 600 °C. Figure 3(b) shows in detail the NBG emission spectral region.

The CLS measurements also show that the NBG transition appears at lower energy than that of standard GaAs. The NBG energy shift is shown in figure 3(b) as a function of electron beam energy for LT GaAs annealed for 10 minutes at 425 °C. The energy shift becomes smaller towards the specimen surface, as shown by the increasing surface sensitive CL spectra. Clearly, part of the excess As can segregate and evaporate from the LT GaAs when annealed in UHV without As overpressure. Assuming that the shifts in NBG emission energy are solely due to changes in the semiconductor lattice constant we can estimate the magnitude of the lattice expansion. Multiplying the bulk modulus, B , and the pressure dependence of the direct energy gap, E_g , we have

$$D = B \cdot (dE_g / dP)_T = -V \cdot (dE_g / dV)_T ,$$

where V is the specimen volume, and P is the applied hydrostatic pressure. Using the experimental values of B , 1.26×10^{-5} eV/bar, and dE_g/dP , 7.54×10^5 bar for GaAs,¹⁸ we obtain for the change in lattice constant a :

$$da/a = 3.6 \times 10^{-5} \cdot dE_g ,$$

where dE_g is the difference in meV between the NBG emission of standard MBE GaAs and that of LT GaAs. We can see that optical techniques are extremely sensitive to lattice constant changes, i. e., a change in 5 meV in band gap energy, easily detected even for optical measurements performed at room temperature,

corresponds to a relative change in lattice constant of 0.017%. The measured dE_g from various experiments range between 30 and 80 meV. Thus, we obtain a relative change in a of 0.1 - 0.3 %. These results agree with X-ray measurements.²

CLS measurements performed on post-growth 600 °C annealed LT GaAs, depicted in figure 3(a), show very poor luminescence intensity, with negligible and featureless emission from deep levels. The CL spectrum also shows a NBG emission energy which is slightly smaller than that of standard GaAs. This indicates that the lattice is still about 0.03 % expanded. CL measurements of *as-grown* LT GaAs annealed at temperatures above 450 °C show similar spectral characteristics: extremely low luminescence signal and substantial reduction in deep level emissions. TEM measurements indicate that the formation and growth of As clusters is occurring at this temperature.¹⁹ Thus, taking into account the relatively intense 1 eV luminescence signal observed in pre-annealed LT GaAs and in LEC GaAs,^{12,20} which indicates a high cross section for deep level radiative recombination, and reported trapping times which are in the picosecond range,²¹ we conclude that the CL measurements performed on post-growth 600 °C annealed LT GaAs show a dramatically reduced concentration of deep level states. These results are consistent with infrared absorption measurements, which show no EL2 absorption,⁸ and EPR measurements, which show defect densities reduced below the resolution limit of about 10^{18} cm^{-3} upon annealing at 600 °C.^{2,6}

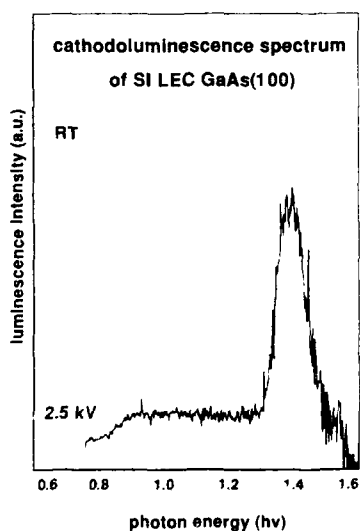


Figure 4. CL spectrum of SI LEC GaAs

Finally in figure 4 we show a CL spectrum of SI LEC GaAs. Previous to insertion in the UHV chamber this sample was etched with a solution of H_2SO_4 and H_2O_2 for 2 minutes, and rinsed with NH_4OH and de-ionized H_2O . This treatment eliminates any chemical and mechanical damage resulting from wafer processing. The spectrum shows a broad and featureless optical emission from deep levels. These deep level emissions are more intense, roughly by a factor 5, than those reported above for post-growth annealed LT GaAs. Moreover, the NBG emission intensity is about 20 times larger than that of annealed LT GaAs. There is no space here to speculate on the physical meaning of this observation. Following Warren et al.,⁶ we may also speculate that a reduced number of As precipitates-recombination centers in SI LEC GaAs will increase the probability of NBG radiative recombination.

CONCLUSIONS

In conclusion, using optical emission techniques we have characterized both pre-annealed and post-annealed LT MBE GaAs. The pre-annealed material shows intense deep level emissions which are associated with the excess concentration of

Arsenic found in LT GaAs. These emissions are assigned to transitions involving As-antisite defects and the VB. These emissions subside with annealing for a few minutes at temperatures above 450 °C, indicating the "healing" of those defects. Concurrently, the excess As diffuses and precipitates into large clusters, forming a large number of buried As/GaAs interfaces. The post-growth 600 °C annealed material shows a dramatically reduced concentration of deep level states. Thus, these results support the "buried" Schottky barrier model of insulation for LT GaAs, e.g. the mechanism of insulation is determined by the properties of the As precipitates and their GaAs/As interfaces.

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PHOTOREFLECTANCE AND X-RAY PHOTOELECTRON SPECTROSCOPY IN LT MBE GaAs

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ABSTRACT

It has recently been shown that a 1000Å cap layer of molecular beam epitaxial (MBE) GaAs grown at 200°C passivates the surface of a GaAs active layer ($n \approx 2 \times 10^{17} \text{cm}^{-3}$) in the sense of reducing the free-carrier depletion which arises from surface acceptor states. The same phenomenon holds for active-layer concentrations up to $7 \times 10^{18} \text{cm}^{-3}$, for caps as thin as 14Å, and for either As₂ or As₄ anion species. In an attempt to understand these effects, we have applied photoreflectance (PR) and x-ray photoelectron spectroscopy (XPS). In general, the PR shows contributions from the surface, cap/active-layer interface, and active-layer/buffer-layer interface, because each of these regions can have a different electric field. In fact, the various field strengths can be determined from Franz-Keldysh oscillations (FKO), and good agreement with Hall-effect measurements is usually found. However, for 200°C material, no PR is seen, suggesting that there is no surface charge (no surface acceptor states below the Fermi level) or at least no surface-charge modulation by the light. The XPS data, which arise only from the near-surface ($\sim 30\text{\AA}$) region, show that the binding energies in the capped samples are increased (i.e., surface Fermi pinning energy decreased) by 0.2 eV with respect to those in the uncapped samples. These data are discussed in relation to a passivation model.

INTRODUCTION

Although the first applications of low-temperature molecular-beam epitaxial (LTMBE) GaAs used the material as a buffer layer underneath an active layer, more recent applications, such as the metal-insulator-semiconductor field-effect transistor (MISFET) and the photoconductive (PC) switch, have used it as a cap layer, on top of the active layer or the substrate [1,2]. Furthermore, the material may have a role simply as a passivation layer, since it is known to reduce free-carrier depletion in the active layer and to enhance the surface breakdown voltage. Thus, it is important to know how the bulk states, surface states, and interface states in the cap interact with the donor states in the active layer. We have earlier used the Hall effect [3] to investigate this problem, and in this work we report, for the first time, the application of x-ray photoelectron spectroscopy (XPS) and photoreflectance (PR) spectroscopy. We also solve the Poisson equation for various possible models to see which ones are consistent with the experimental data.

SAMPLES

In this study, we will primarily deal with five, representative samples, grown sequentially in a Varian Gen II apparatus over the course of a single day, and each having the following basic structure: (1) a 650μm, Si GaAs substrate; (2) a 5000Å, undoped buffer layer, grown with As₂ at 580°C; and (3) a 2500Å, Si-doped active layer, grown with As₂ at 580°C and having $n \approx N_{\text{da}} \approx 2.4 \times 10^{17} \text{cm}^{-3}$. Four of the samples were then capped with a 1000Å layer grown at 200 or 400°C, and with As₂ or As₄, as enumerated in Table I; the fifth sample was left uncapped, as a control. Numerous other LTMBE GaAs samples, grown under similar conditions, basically produce the

Table 1. Characteristics of samples used in this study. $E_{Fs} = E_C - E_F$ at the surface.

Cap growth T	Cap As species	Δn^{sh} -Hall (10^{12}cm^{-2})	Δn^{sh} -PR (10^{12}cm^{-2})	ΔE_{Fs} -XPS (eV)
no cap		0	0	0
200°C	As ₂	1.15	no surf signal	-0.18
400°C	As ₂	1.48	0.95	-0.04
200°C	As ₄	0.54	no surf signal	-0.18
400°C	As ₄	0.95	0.95	+0.01

same Hall, XPS, and PR results as will be reported here. The one exception is sample 2 (200°C, As₂), which has a higher sheet electron concentration than has been measured in other, similar samples. This point is discussed later.

THEORY

Some possible conduction-band diagrams which will fit the Hall data are given in Fig. 1. These curves result from numerical solutions to the one-dimensional Poisson equation with the parameters given in Table 2, and it can be seen that those parameters give sheet free-electron concentrations n^{sh} which are consistent with the measured ones. Furthermore, the given parameters correctly predict Δn^{sh} as the cap thickness d_c is reduced by etching, as discussed in detail elsewhere. The surface states N_{as} were chosen to be acceptors of sheet density $1 \times 10^{13} \text{cm}^{-2}$ and energy $E_c - 0.7 \text{ eV}$, since these values

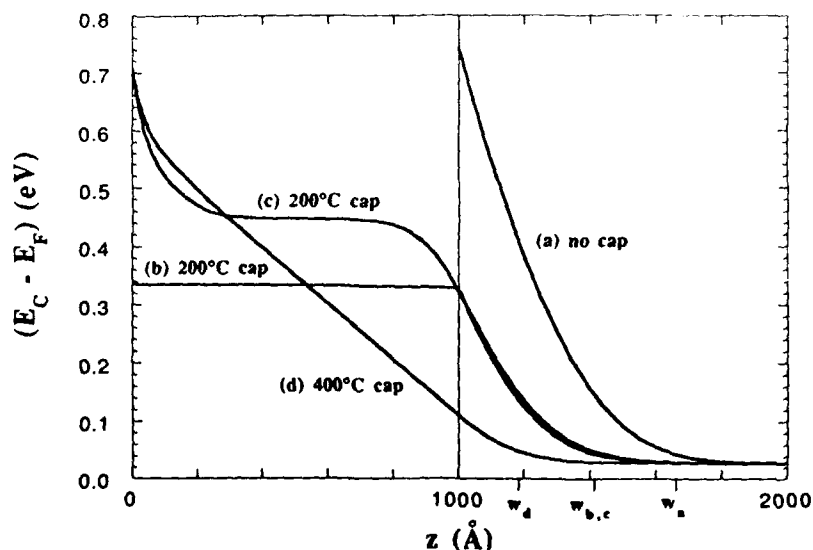


Fig. 1. Conduction band diagrams for various cap characteristics. The w_i 's are effective depletion lengths.

Table 2. Parameters used to compute the various curves in Fig. 1. Superscript "sh" denotes a sheet density.

Curve	N_{As}^{sh} (10^{13} cm^{-2})	N_{Ai}^{sh} (10^{11} cm^{-2})	N_{Ac} (10^{18} cm^{-3})	N_{Dc1} (10^{19} cm^{-3})	N_{Dc2} (10^{18} cm^{-3})	Δn^{sh} (10^{12} cm^{-2})
(a) no cap	1.0	N/A	N/A	N/A	N/A	0
(b) 200°C, As ₄	0	9.5	0.001	3.0	0	0.56
(c) 200°C, As ₄	1.0	0	1.0	3.0	2.0	0.50
(d) 400°C, As ₄	1.0	1.0	0.001	*3.0	0	1.06

*actually unknown, but less than $3 \times 10^{19} \text{ cm}^{-3}$

agree well with those in the literature, and tend to pin E_{fs} at $E_c \sim 0.7 \text{ eV}$. The interface states were chosen to be near the valence band (E_v to $+0.1 \text{ eV}$) since there is evidence that they may be carbon related, arising from impurities adsorbed during growth interruption as the wafer is cooled from 580 to 200 or 400°C. The concentration of acceptors N_{ac} in the volume of the cap is somewhat controversial at present, with EPR results [4] favoring a value greater than 10^{18} cm^{-3} , and the original Hall results [5] predicting a lower value of $1 \times 10^{15} \text{ cm}^{-3}$. However, we have recently shown that if the substrate contribution to the Hall coefficient is taken into account, then the Hall data can also be fitted with N_{ac} greater than 10^{18} cm^{-3} . With respect to the donors, there is general agreement that an arsenic-antisite related center (N_{dc1}) is present at very high concentrations ($10^{19} - 10^{20} \text{ cm}^{-3}$) in the 200°C samples. Since the absorption signature is very much like that of EL2, it is presumed that the energy of N_{dc1} is at $E_c - 0.75 \text{ eV}$ at $T=0$, and $E_c - 0.65 \text{ eV}$ at $T=296 \text{ K}$. If N_{ac} is greater than $1 \times 10^{18} \text{ cm}^{-3}$, as deduced from EPR results, then it is necessary to either invoke a second donor, shallower than EL2, or a donor interface charge, in order to get the correct sheet Hall concentration (Table 1) for the 200°C, As₄ sample. For example, we can get a good fit by assuming $N_{dc2} \approx 2 \times 10^{18} \text{ cm}^{-3}$ and $E_{dc2} \approx E_c - 0.43 \text{ eV}$ at 296 K. However, E_{dc2} could be deeper if a donor interface charge is also present. In the rest of the paper these models are examined with respect to XPS and PR data.

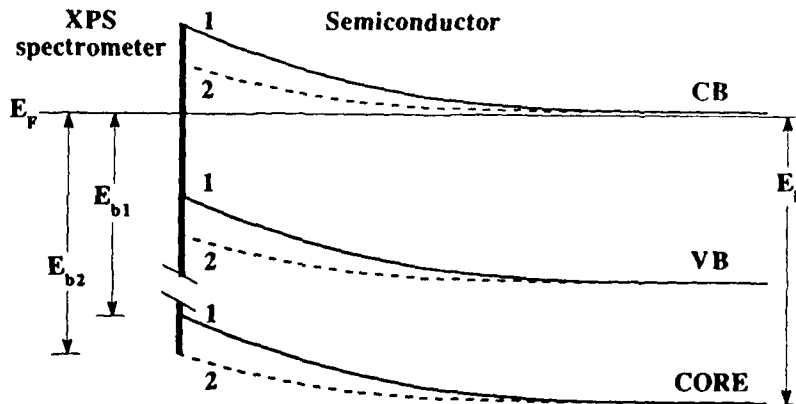


Fig. 2. Surface (E_{b1} and E_{b2}) and bulk (E_b) binding energies for two band-bending conditions

X-RAY PHOTOELECTRON SPECTROSCOPY

The XPS data were taken on a Surface Science Instruments M-Probe operating with the monochromatic $Al_{K\alpha}$ line at $E_x = 1486.6$ eV. The instrument measures the kinetic energy E_k of the emitted photoelectrons, and since $E_k = E_x - E_b - \phi$ (the spectrometer work function), it is easy to get E_b , the binding energy with respect to the Fermi energy. In Fig. 2 we schematically show an n-type semiconductor, in equilibrium with an XPS apparatus, for two different cases of semiconductor band bending. For case 2 the band bending is smaller, which means the binding energy ($E_f - E_{core}$) at the surface is larger. Thus, if the surface is passivated (smaller band bending) then E_b will be larger.

For samples which are not strongly conducting, such as the 400°C-capped layers, the apparent energies can be shifted due to charging effects. To minimize this problem, we used a neutralizing screen in front of the samples and out of focus with the analyzer. To further correct for charging effects, all As and Ga lines in a particular sample were referenced to the carbon 1s line (evidently surface carbon) in that sample. In Fig. 3 are presented the As 3d spectra for the control sample (no cap), and the 200°C, As_4 -capped sample. Clearly, the capped sample spectrum is shifted to a higher binding energy (lower band bending). The spectra were fitted with Gaussian functions, after removing an integral (Shirley) background, in two different ways — assuming (1) that each line was a singlet, or (2) a spin-orbit-split doublet. The As 3d singlet results are presented in Table I, and are consistent: both 200°C-capped samples shift about 0.2 eV to higher binding energy (lower band bending), and both 400°C-capped samples exhibit only a small shift, possibly insignificant with respect to the error in the energy determinations.

We now compare these results with the various models represented by conduction-band diagrams in Fig. 1. Since the average emission depth of the photoelectrons is only about 15 Å, the relevant binding energy is that very close to the surface. Thus, the XPS results predict an equal or slightly smaller surface potential for curve (d) (400°C, As_4) with respect to curve (a) (no cap), and that indeed is the case. For the 200°C samples, the XPS data would predict a surface potential of about $0.7 - 0.2 = 0.5$ eV, right between the curve (b) and curve (c) values. Thus, it appears that neither model is exactly correct. However, it is clear that the surface Fermi-level cannot be pinned at $E_c - 0.7$ eV (curve (c)) and still be consistent with the XPS data unless the surface depletion width is less than 15 Å, so that $E_c - E_f$ would be averaged from 0.7 to 0.4 eV. For this to be true, the shallow donor would have to have a concentration of $10^{19} - 10^{20}$ cm⁻³, in order to accommodate 10^{13} cm⁻² surface acceptors in 15 Å. A donor deeper than 0.4 eV could also be allowed if it were accompanied by an interface donor charge, but it still would have to be shallow enough to produce a

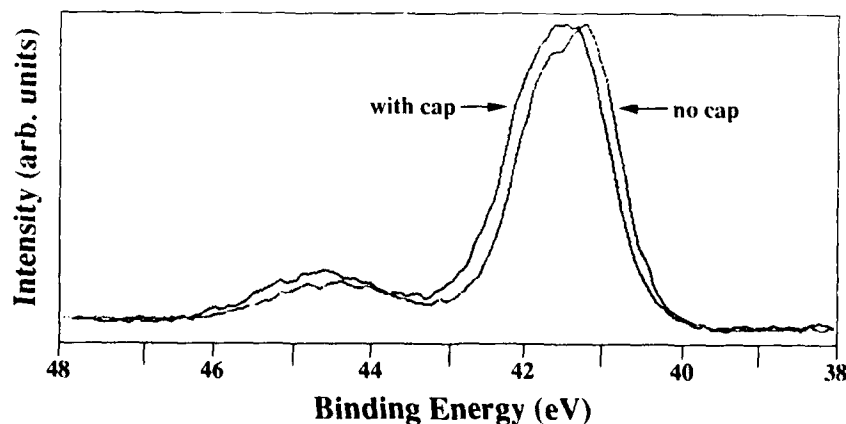


Fig. 3. XPS As 3d lines for samples with and without a 200°C, 1000 Å cap.

flat-band (at $E_c - E_f \lesssim 0.5$ eV) in the cap in order to satisfy the XPS data. Different interface donor concentrations could also explain why the Hall concentration differs among samples, such as the As₂- and As₄- capped samples in Table 1.

PHOTOREFLECTANCE SPECTROSCOPY

Photoreflectance (PR) spectra result from the modulation of an electric field (and thus the dielectric constant) by a modulated light source which, in our case, is the 632.8 nm line from an HeNe laser. Since this line can penetrate more than 3500 Å, it can possibly modulate three fields in our samples: (1) the field at the cap surface; (2) the field at the cap/active-layer interface; and (3) the field at the active-layer/buffer-layer interface. The PR data are presented in Fig. 4. The fields can be calculated from the Franz-Keldysh oscillations (FKO) in the usual way. First note that the control sample has three FKO extrema at 830, 794, and 766 nm; these give a field $\mathcal{E} = -1.8 \times 10^5$ V/cm, or a depletion charge $Q = -(\epsilon/e)\mathcal{E} = 1.3 \times 10^{12}$ cm⁻². This agrees satisfactorily with the value $N_{da}w_a = 1.5 \times 10^{12}$ cm⁻² from Hall measurements. Next, the 400°C sample has many extrema in the 757–853 range, leading to $\mathcal{E} \approx -4.9 \times 10^4$ V/cm, or $Q \approx 3.5 \times 10^{11}$ cm⁻². Here the Hall data predicted $Q = 4.8 \times 10^{11}$ cm⁻², again in satisfactory agreement considering the potential errors in the two independent measurements. Finally, the control and 200°C-capped samples have several short-period oscillations between 840 and 880 nm, and the 400°C-capped sample also appears to have them, although they are hidden by the much larger surface oscillations. These short-period FKO lead to a field $\mathcal{E} = -1.7 \times 10^4$ V/cm, which is very close to what is expected from the active-layer/buffer-layer interface (-1.6×10^4 V/cm). Support for this interpretation comes from the fact that these oscillations are absent if the buffer layer is absent. Thus, the PR results are all well understood and consistent with the Hall and XPS results for the control and 400°C-capped samples. The 200°C-capped samples, on the other hand, show no PR signal at all except for the buffer contribution.

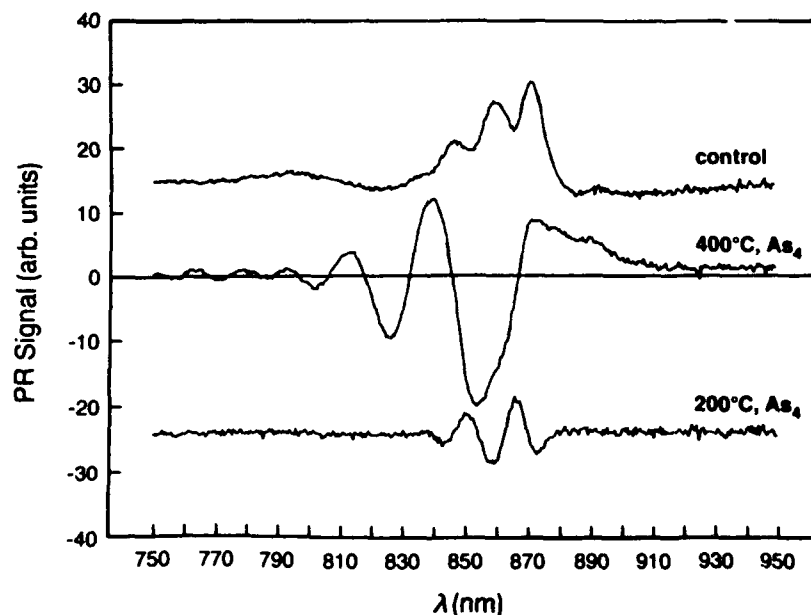


Fig. 4. Photoreflectance data for three samples. The base-line displacements are arbitrary.

The absence of a PR signal from 200°C MBE GaAs most likely arises from one of the following two causes: (1) there are no surface acceptor states to charge up and therefore no surface field; or (2) there is a surface field but the light modulation cannot affect it. The first case would be depicted by curve (b) of Fig. 1; however, then the surface potential as deduced by XPS should have been about 0.35 eV lower than that of the control sample, rather than 0.18 eV. The second case would be represented by curve (c); here, the surface potential would presumably be averaged over the first 10–20 Å of the surface band bending which could well be consistent with the observed 0.18 eV differential if N_{dc2} were large enough. (For example, 10^{20} cm^{-3} deep donor states would compensate 10^{13} cm^{-2} surface acceptor states in 10 Å.) If case 2 is correct, then we still need to explain why the surface field is not modulated. One reason might be that only a small volume of photoexcited holes (i.e., just 10 Å deep) is swept to the surface and is thus available to neutralize negatively charged acceptors. Also, the recombination time might be very short because the bath of free electrons is within 10 Å of the surface and can easily tunnel through the barrier, which is only about 0.3 eV high (0.7–0.43 eV). Contrast this situation with that of the 400°C-capped sample, curve (d), in which the effective photoexcitation volume and barrier are more than 1000 Å thick. Thus, the photoexcited holes should be much more effective in neutralizing surface acceptor states in the latter case.

PASSIVATION MODEL

The passivation (reduction of free-carrier depletion) by a 400°C (or 580°C) cap layer is well understood and results from the surface acceptor states being displaced from the active layer. The passivation by a 200°C cap is not as well understood, but it is clear from Hall/etching experiments that a 200°C cap must have a long, flat-band region. A flat-band can be due to (1) small bulk and surface acceptor concentrations in the cap, or (2) a large bulk acceptor concentration and an even larger bulk donor concentration, which controls the Fermi level. The latter case is more consistent with EPR and recent absorption measurements, but the XPS data suggest that such a donor must be shallower than EL2 by a least 0.1–0.2 eV, even though it may still be related to As_{Ga} .

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ANNEALING CHARACTERISTICS OF LOW TEMPERATURE GROWN GaAs:Be

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ABSTRACT

We have studied the annealing characteristics of acceptor doped GaAs:Be grown at Low substrate Temperatures (300°C) by Molecular Beam Epitaxy (LTMBE). The Be was introduced in a range of concentrations from 10^{16} - 10^{19} cm⁻³. As-grown material was found to be n-type even up to the highest Be concentration of 10^{19} cm⁻³ although Raman spectroscopy of the Be local vibrational mode indicates that the majority of the Be impurities are substitutional. We propose that Be acceptors are rendered inactive by the high concentration of As_{Ga}-related native donor defects present. Results of slow positron annihilation studies indicate an excess concentration of V_{Ga} in LTMBE layers over bulk grown crystals. A distinct annealing stage at 500°C, similar to irradiation damaged and plastically deformed GaAs, marks a rapid decrease in the As_{Ga} defect concentration. A second annealing stage at 800°C corresponds to the activation of Be acceptors. Analysis of isothermal annealing kinetics for the removal of As_{Ga}-related defects gives an activation energy of 1.7 ± 0.3 eV. We model the defect removal mechanism with the V_{Ga} assisted diffusion of As_{Ga} to As precipitates.

INTRODUCTION

More than a decade ago it was proposed [1] that GaAs grown at low temperatures, ~400°C, would make an excellent buffer layer for field effect transistors. Recently it was found that lowering the buffer layer growth temperature even further, ~200-300°C, resulted in substantial performance improvements for GaAs integrated circuits [2]. It is this novel material grown at 200-300°C that we shall refer to as LTMBE GaAs which has generated great technological and scientific interest.

Of great scientific interest is the extremely high quantity of excess As, ~1.5% [3]. The excess As is incorporated mainly as As_{Ga}-related defects [4] in as-grown material and as arsenic precipitates after annealing [5]. The extremely high concentrations of native defects in as-grown material provide a unique opportunity to study the reactions between native defects and/or intentionally introduced impurities in highly non-stoichiometric material.

The high resistivity $\sim 10^4$ to 10^5 Ωcm, of LTMBE GaAs has been attributed to the high concentration of excess As. As grown, however, these materials exhibit conductivity characteristics of a hopping mechanism via defects [6]. Only after annealing the layers at temperatures above 500°C, such as encountered during the subsequent growth of a standard MBE layer, does the material become Semi-Insulating (SI) with resistivities $\sim 10^7$ Ωcm.

Because of the practical importance of LTMBE GaAs buffer layers, most studies have been of undoped materials. However, a recent study of the dependence of Si donor doping efficiency on the stoichiometry of LTMBE GaAs layers shows that any significant non-stoichiometric deviation towards arsenic rich material always leads to reduced activity of Si donors [7]. Some attention has been paid to the effects of growth temperature on the efficiency of p-type doping [8].

The aim of the present study is to shed light on the properties of defects and defect-impurity reactions in p-type doped LTMBE GaAs. We investigate the thermal stability of defects in GaAs doped with Be in a wide concentration range. Also we have determined the annealing conditions required to activate Be acceptors in LTMBE GaAs. A model has been proposed [9] which describes annealing of As_{Ga}-related defects via gallium vacancy assisted diffusion.

EXPERIMENTAL

Samples were grown in a Varian Gen II MBE system. The substrates were (100) SI LEC GaAs wafers. The growth was initiated at a substrate temperature of 580°C, depositing 100Å of conventional MBE GaAs, before ramping down to a temperature of 300°C and growing 3μm of LTMBE GaAs. The surface was As stabilized with an As₄/Ga flux ratio of 2. The growth rate for

the layers was $1\mu\text{m hr}^{-1}$. Be concentrations of 10^{16} , 10^{17} , 10^{18} , and 10^{19} cm^{-3} were introduced in a series of samples.

Electrical measurements were made using a high impedance Hall effect system with samples in the van der Pauw geometry. Ohmic contacts were alloyed with pure In at 200°C for 4 minutes.

IR absorption measurements were made using a Cary 2300 spectrophotometer. Neutral EL2 like defect concentrations are estimated from the absorption at a wavelength of $1\mu\text{m}$ relative to the background absorption at $1.7\mu\text{m}$ using the calibration of Martin [10].

Positron annihilation studies were performed with a variable energy positron beam at the Institute of Materials Science, Tsukuba, Japan. The relative V_{Ga} concentrations were determined from the S-parameter characteristic of the Doppler broadened 511 keV annihilation γ -ray [11]. S is defined as the ratio of the number of central region counts to total counts. The central region was chosen from 510.5 to 511.5 keV and the total number of counts at all energies was 5×10^5 .

Samples were annealed isochronally for 20 minutes at 330, 370, 415, 470, 550, 625, 700 and 800°C . Below 500°C the samples were annealed in flowing N_2 . Above 500°C the samples were sealed in an evacuated ampoule with enough elemental As to maintain an overpressure of 2 atm. at the annealing temperature to prevent As loss.

Isothermal anneals were performed at 430, 450 and 490°C in flowing N_2 . During the course of annealing, the samples were removed at specific time intervals to make room temperature IR absorption measurements and then were placed back in the furnace.

RESULTS AND DISCUSSION

As-grown LTMBE layers

Figure 1 shows IR absorption spectra recorded at 10K. Spectra (a, b, c, d) of all four as-grown Be doped samples are shown. Spectrum (e) belongs to of the 10^{18} cm^{-3} doped sample taken after a 30 minute white light illumination and illustrates the photoquenching properties of these layers. Spectrum (f) is the ratio before and after illumination showing the photoquenchable (PQ) IR absorption. All the spectra show a characteristic broad absorption at 1.2 eV similar to EL2 but no zero phonon line near 1.04 eV is visible. The PQ fraction of defects ranged from 60% to 85%. The highest concentration of neutral As_{Ga} is $3 \times 10^{19}\text{ cm}^{-3}$ for the 10^{17} cm^{-3} doped sample. Increased Be doping reduced the concentration of neutral As_{Ga} -related defects to $1.5 \times 10^{19}\text{ cm}^{-3}$. If we consider the donor like As_{Ga} -related defects to be compensated by Be, then the total concentration $[\text{As}_{\text{Ga}}]$ for the $[\text{Be}] = 10^{19}\text{ cm}^{-3}$ doped sample would be $2.5 \times 10^{19}\text{ cm}^{-3}$. This indicates that the total $[\text{As}_{\text{Ga}}]$ remains roughly constant and does not depend on the $[\text{Be}]$.

One striking aspect of electrical measurements of our as-grown LTMBE GaAs:Be is the lack of p-type conductivity. Figure 2 shows results of temperature dependent resistivity measurements for the as-grown sample doped with $[\text{Be}] = 10^{17}\text{ cm}^{-3}$. Both this and the sample doped with $[\text{Be}] = 10^{16}\text{ cm}^{-3}$ exhibit n-type conductivity. Unfortunately in the two more highly doped samples ($[\text{Be}] = 10^{18}$ and 10^{19} cm^{-3}), the first 100Å of standard GaAs were inadvertently Be doped. This created a shunting layer at the interface making electrical studies of these LTMBE layers impossible. However, it did not affect optical measurements of these layers.

The temperature dependence of the resistivity ρ (see Fig. 2) can be expressed as

$$\frac{1}{\rho} = \frac{1}{\rho_1} \exp\left[-\frac{\epsilon_1}{kT}\right] + \frac{1}{\rho_3} \exp\left[-\frac{\epsilon_3}{kT}\right], \quad (1)$$

where k is Boltzman's constant and T is the temperature. ρ_1 and ϵ_1 are the extrapolated infinite temperature intercept and the activation energy of the resistivity above room temperature and correspondingly ρ_3 and ϵ_3 describe the resistivity below room temperature.

Above room temperature the activation energy for the resistivity is $\epsilon_1 = 0.75\text{ eV}$. This is representative of the normal free carrier conduction due to the thermal excitation of electrons to the conduction band from the Fermi energy pinned to the defect level at midgap. Below room temperature the conductivity mechanism has been proposed to be the thermally assisted hopping of electrons via localized As_{Ga} -related defect states [6]. We find the activation energy ϵ_3 to be $75 \pm 3\text{ meV}$ and $92 \pm 3\text{ meV}$ for the samples doped 10^{16} and 10^{17} cm^{-3} respectively.

An important question is whether the Be impurities are substitutional in as-grown layers. We have previously [9] measured the Raman spectrum of the Be local vibrational mode in as-grown LTMBE GaAs heavily doped, 10^{19} cm^{-3} , with Be. Our results indicate that a significant fraction

of the total Be, greater than 50%, must occupy substitutional positions. Therefore, the Be must either be compensated by native defects or form complexes with them.

Another point defect accommodating excess As in GaAs, besides the As_{Ga} , is the V_{Ga} . Positron annihilation experiments were performed to determine the relative $[V_{Ga}]$ as a function of Be doping. The magnitude of the S-parameter is a measure for the $[V_{Ga}]$, with a larger value of S indicating a higher $[V_{Ga}]$. More detailed discussions of slow positron annihilation measurements and Doppler broadened γ ray spectroscopy can be found in the literature [11].

The results of the positron annihilation experiments are shown in Fig. 3. The LEC substrate gives the lowest S parameter and thus has the lowest V_{Ga} concentration. LTMBE layers exhibit a larger S parameter which indicates that a larger concentration of V_{Ga} are present. Note that a larger $[V_{Ga}]$ is found in the lightly doped (10^{16} cm^{-3}) layer than in the heavily doped (10^{19} cm^{-3}) layer. This trend is understandable as one expects lower concentrations of negatively charged $[V_{Ga}]$ with Be acceptors present. Although we cannot quantify the positron annihilation results they provide us with very important information about the presence of $[V_{Ga}]$ in LTMBE GaAs.

Annealed LTMBE layers

Figure 4 shows the IR absorption at a wavelength of 1.24 eV versus anneal temperature. The filled-in symbols connected by solid lines represent the total neutral defect absorption taken at 10K before illumination. The open symbols connected by dashed lines represent the PQ portion of the absorption. The obvious feature of Fig. 4 is the distinct annealing stage between 470 and 550°C corresponding to a large decrease in the total IR absorption. For temperatures less than 430°C, it appears that the non-PQ defects are thermally less stable than the PQ defects. For the 10^{16} and 10^{18} cm^{-3} doped samples the PQ absorption even increases. The slight increase in PQ absorption could indicate that some of the non-PQ defects are being converted into PQ defects.

The dependence of the electrical properties on the anneal temperature was also investigated. The temperature dependent resistivity of the $[Be] = 10^{17} \text{ cm}^{-3}$

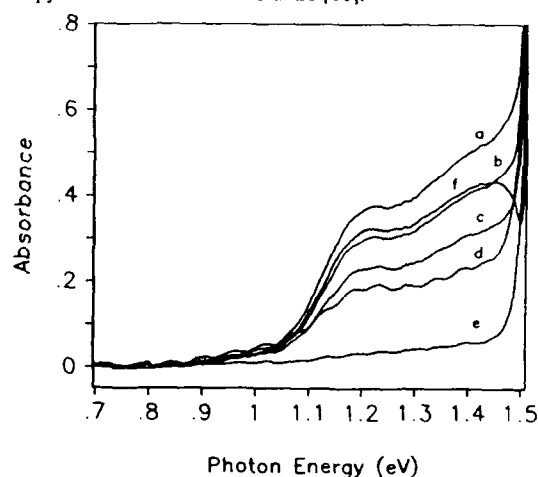


FIG. 1. IR absorption spectra of LTMBE GaAs:Be layers corrected for substrate absorption. a. 10^{17} cm^{-3} doped layer, b. 10^{16} cm^{-3} , c. 10^{18} cm^{-3} , d. 10^{19} cm^{-3} , e. 10^{18} cm^{-3} doped layer after 30 min. white light illumination, f. PQ absorption of 10^{17} cm^{-3} doped layer given by the ratio of spectra taken before and after illumination.

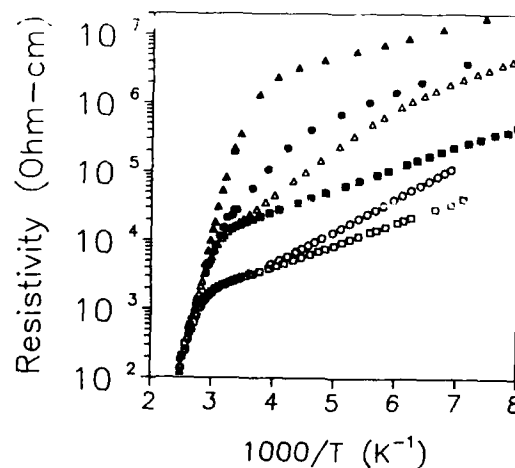


FIG. 2. Temperature dependent resistivity of isochronally annealed samples. Annealing time was 20 minutes. Initial steep slope is parallel conductivity of substrate. Shallower low temperature slope is thermally activated hopping conduction. Hopping conductivity is reduced in annealed samples. Annealing temperatures were: (O) as grown, (□) 330°C, (Δ) 370°C, (■) 415°C, (●) 470°C, (▲) 550°C.)

doped sample is shown in Fig. 2 for anneals up to 550°C. The resistivity of the annealed sample can also be described by equation (1). For increasing annealing temperatures, the region described by ρ_3 and ϵ_3 moves towards higher resistivity. The resistivity at 250 K increases nearly 3 orders of magnitude after annealing at 550 K. For the same annealing temperature, the defect concentration decreases by only a factor of 8 (see Fig. 4). This strong dependence of the resistivity on the defect concentration is further evidence for a hopping conduction mechanism. It reflects the exponential dependence of the electron wavefunction overlap on the hopping center separation.

One important point to note is that only after annealing at 800°C does the sample become p-type. Although the As_{Ga} -related donors rapidly anneal off at 550°C we do not observe any electrical activity of Be acceptors below 700°C. Since our Raman scattering experiments show that most of the Be atoms are substitutional we have to conclude that a large concentration of As_{Ga} defect-related donors is stable up to 700°C. A possible explanation for the enhanced stability of the donors is that they form complexes with substitutional Be acceptors. For the next nearest neighbor pair, $\text{As}_{\text{Ga}}^+ + \text{Be}_{\text{Ga}}^-$, the electrostatic attraction energy is about 1.2 eV. Ionized As_{Ga}^+ defects tied up in the pairs do not contribute to IR absorption and cannot be detected in absorption measurements. The activation of Be acceptors at temperatures exceeding 700°C is associated with a break up of $\text{As}_{\text{Ga}}^+ + \text{Be}_{\text{Ga}}^-$ pairs and subsequent diffusion of As_{Ga} to As precipitates.

Isothermal annealing studies were performed to better understand the kinetics of the As_{Ga}

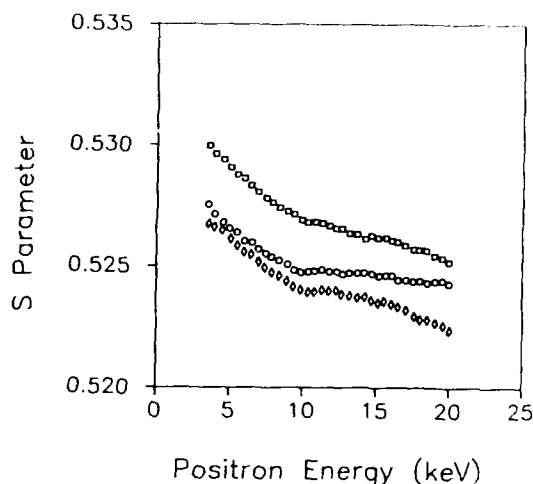


FIG. 3. Results of slow positron Annihilation measurements. S parameter vs. positron energy. Larger S parameter indicates higher V_{Ga} concentration. (○) Si LEC GaAs substrate, (□) LTMBE GaAs:Be 10^{19} cm^{-3} , (◻) LTMBE GaAs:Be 10^{17} cm^{-3} .

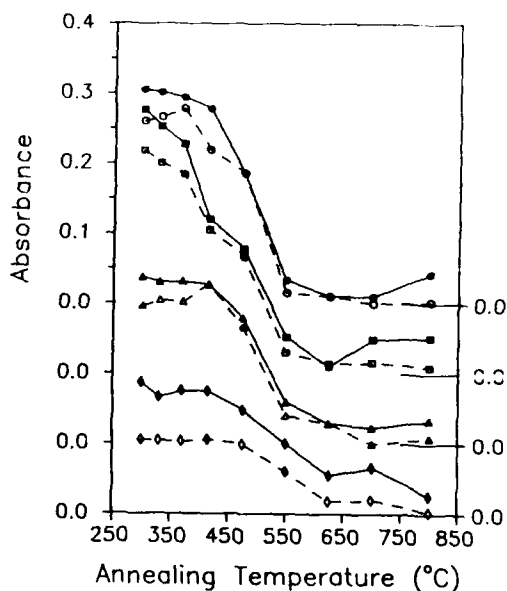


FIG. 4. Dependence of 10K IR absorption at 1.24 eV on isochronal annealing temperature. Filled in symbols are for the total neutral defect absorption before illumination. Open symbols are the ratio of absorption before/after 30 minute white light illumination, representing the photoquenchable portion of the defect absorption. (●) $[\text{Be}] = 10^{16} \text{ cm}^{-3}$, (■) $[\text{Be}] = 10^{17} \text{ cm}^{-3}$, (▲) $[\text{Be}] = 10^{18} \text{ cm}^{-3}$, (◆) $[\text{Be}] = 10^{19} \text{ cm}^{-3}$.

annealing stage at 500°C. The dependence of the IR absorption at 1 μ m on the annealing time is plotted in Fig. 5 which shows the recovery transient at 490°C of the four differently doped samples. The solid lines are fits to the annealing transients. The dependence of the measured absorption A as a function of time t is given by:

$$A = A_0 + A_1 \exp\left[-\frac{t}{\tau}\right] \quad (2)$$

where A_0 , A_1 , and τ are the fit parameters. An Arrhenius plot of τ is shown in Fig. 6 for the four doping levels. The samples can be broken into two groups. The two heavily doped samples give one set of values for τ and the lightly doped samples another. For increasing Be doping the general trend is that τ becomes larger, but the activation energy of the recovery remains approximately constant. We find an activation energy of 1.7 ± 0.3 eV indicated by the dashed line in Fig. 6. This value for the defect annealing activation energy in LTMBE GaAs is similar to the 1.6 eV found in fast neutron irradiated GaAs [12].

We find that in LTMBE most of the As_{Ga} -related defects anneal very rapidly at about 500°C. This behavior is similar to the annealing characteristics of EL2 in GaAs heavily damaged by plastic deformation [13], or fast neutrons [14]. In stark contrast, EL2 defects in as-grown bulk GaAs crystals are much more stable and anneal away only at temperatures higher than 1000°C. The difference in the annealing behavior has led to suggestions that the EL2-like defects in heavily damaged GaAs are defect complexes rather than isolated As_{Ga} defects. We would like to argue here that it does not have to be the case.

Our positron annihilation results indicate the presence of V_{Ga} in LTMBE. In addition, it has been shown that large concentrations of V_{Ga} exist in neutron [15] irradiated GaAs. Therefore, we propose that the presence of V_{Ga} acceptors enhances the low temperature ($\sim 500^\circ\text{C}$) annealing of As_{Ga} -related defects. Mobile V_{Ga} assist the diffusion of As_{Ga} in a site exchange process,

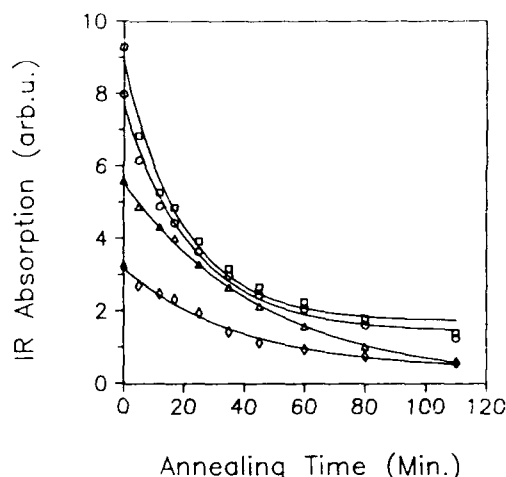


Fig. 5. Isothermal annealing transients of the 1.24 eV IR absorption at 490°C. Symbols are the experimental points. Solid lines are fits of Eq. (2) to the data. (\circ [Be] = 10^{16} cm^{-3} , \square [Be] = 10^{17} cm^{-3} , \triangle [Be] = 10^{18} cm^{-3} , \diamond [Be] = 10^{19} cm^{-3})

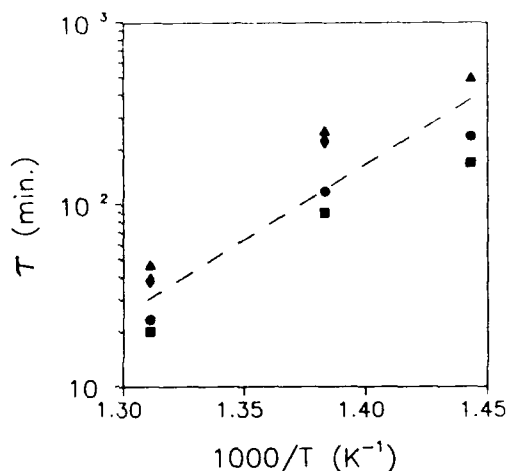


Fig. 6. Arrhenius plot of the recovery time constant fit parameter for the various doped samples. The activation energy of the recovery process is approximately the same for all dopings, 1.7 ± 0.3 eV, as indicated by the dashed line. The pre-exponential of the recovery kinetics depends on doping. (\bullet [Be] = 10^{16} cm^{-3} , \blacksquare [Be] = 10^{17} cm^{-3} , \blacktriangle [Be] = 10^{18} cm^{-3} , \blacklozenge [Be] = 10^{19} cm^{-3})

where 1 and 2 denote two different next nearest neighbor Ga sites. The As_{Ga} defects are annihilated upon encountering an As precipitate. Since the V_{Ga} already exist in the material, only the energy of migration, E_m must be overcome for As_{Ga} diffusion to occur.

In contrast, the concentration of V_{Ga} in bulk GaAs grown under equilibrium conditions is quite low. Theoretical calculations [16] estimate the $[V_{Ga}]$ in stoichiometric undoped SI material to be $\sim 5 \times 10^{14} \text{ cm}^{-3}$. For diffusion to occur in bulk materials, V_{Ga} must be created first. Both the energy of migration, E_m and now the energy of formation, E_{fv} for V_{Ga} must be overcome. Recent theoretical calculations [16] for V_{Ga} in As rich SI GaAs give $E_{fv} = 2.5 \pm 0.5 \text{ eV}$. Interpreting the activation energy we measure as the migration energy, $E_m = 1.7 \pm 0.3 \text{ eV}$, the sum gives an activation energy for diffusion in bulk GaAs of $4.2 \pm 0.8 \text{ eV}$. Therefore, As_{Ga} diffusion in bulk material requires a much higher temperature than for damaged materials in order to create V_{Ga} .

A semi-empirical model which calculates the $[V_{Ga}]$ necessary to promote the diffusion of As_{Ga} to As precipitates has been proposed concurrently [9]. The model considers spherically symmetric diffusion of As_{Ga} to a precipitate of radius r_0 , within a finite volume defined by a sphere of radius R which is half the mean spacing between precipitates. The assumptions of the model are that the precipitate is an infinite sink, the gradient of the As_{Ga} concentration half way between precipitates is zero, and that the diffusivity is constant. This last assumption is only valid for short annealing times. The supersaturated $[V_{Ga}]$ will be decreasing during the course of the annealing so that the diffusion process will slow down. Experimental values taken from Fig. 6 for the 490°C isothermal annealing of the 10^{17} cm^{-3} doped sample are $\tau = 20 \text{ min}$ and $\Delta H_m = 1.7 \text{ eV}$. Typical values of r_0 and R determined from microscopy studies of precipitates in the layers are $\sim 20 \text{ \AA}$ and 100 \AA respectively. The concentration of V_{Ga} is calculated to be $\sim 10^{19} \text{ cm}^{-3}$.

This concentration of V_{Ga} given by the model is consistent with EPR measurements which have shown that $\sim 5 \times 10^{18} \text{ cm}^{-3}$ of paramagnetically active As_{Ga}^+ can exist in LTMBE GaAs [4].

CONCLUSIONS

We have investigated the properties of as-grown and annealed LTMBE GaAs:Be. These materials contain a high concentration of excess As which is incorporated in as-grown material as point defects, mainly As_{Ga} and to a lesser extent V_{Ga} . After annealing, the excess As is predominantly in the form of As precipitates. The Be occupies substitutional sites but is compensated by the high concentration of point defects even up to $[Be] = 10^{19} \text{ cm}^{-3}$.

Two distinct defect annealing stages were found in these materials. At 500°C , the PQ As_{Ga} -related defects anneal away. Finally, after annealing at 800°C , holes are activated to the valence band. In addition, at 330°C , non-PQ As_{Ga} -related defects begin to anneal away. These annealing stages are similar to annealing stages in other defect containing GaAs materials.

For the annealing stage at 500°C , the activation energy was found to be $1.7 \pm 0.3 \text{ eV}$. A model of the annealing process as V_{Ga} enhanced diffusion of As_{Ga} to precipitates is consistent with the experimental results and explains the lower thermal stability of As_{Ga} defects in LTMBE GaAs.

ACKNOWLEDGEMENTS

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PART II

Structural Properties of LT GaAs

CRYSTAL STRUCTURE OF LT GaAs LAYERS BEFORE AND AFTER ANNEALING

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ABSTRACT

The structural quality of GaAs layers grown at low temperatures by solid-source and gas-source MBE at different growth conditions is described. Dependence on the growth temperature and concentration of As [expressed as As/Ga beam equivalent pressure (BEP)] used for the growth is discussed. A higher growth temperature is required to obtain the same monocrystalline layer thickness with increased BEP. The annealing of these layers is associated with the formation of As precipitates. Semicoherent precipitates with lowest formation energies are formed in the monocrystalline parts of the layers grown with the lowest BEP. Precipitates with higher formation energies are formed when higher BEP is applied; they are also formed in the vicinity of structural defects. Formation of As precipitates releases strain in the layers. Arsenic precipitates are not formed in annealed ternary (InAlAs) layers despite their semi-insulating properties. The role of As precipitates in semi-insulating properties and the short lifetime of minority carriers in these layers is discussed.

INTRODUCTION

GaAs layers grown by molecular-beam epitaxy (MBE) at very low temperatures ($\sim 200^\circ\text{C}$) (LT) have gained considerable interest as buffer layers for GaAs metal-semiconductor field effect transistors (MESFETs) due to high resistivity resulting in excellent device isolation.^{1,2} By application of these layers, side gating/back gating can be removed. However, this semi-insulating behavior can be obtained only after annealing. These layers can be applied as well as surface passivation layers. In addition, fast photodetectors can be built based on LT-GaAs, since the minority carrier lifetime in this material is very short (in the range of a few hundred fsec).

Earlier studies by electron paramagnetic resonance combined with optical absorption^{3,4} reveal 10^{20} cm^{-3} As_{Ga} antisite defects in as-grown layers, a defect concentration that decreases at least two orders of magnitude after annealing. These layers are grown from As supersaturation and show up to 1.5% excess As, which leads to $\sim 0.1\%$ of expansion of the lattice parameter. This expansion of the lattice parameter disappears after annealing. An important problem of LT-Layers is the breakdown of single crystal growth that is observed at too low temperature and/or too high As/Ga ratio in the layer. Since usually a device structure is grown on top of the LT-layers, their crystalline perfection is very important.

This paper reviews recent work on the structure of LT-layers, along with new results of a systematic study of different growth and annealing conditions.

GaAs LAYERS GROWN BY MBE

It was noticed earlier that the crystalline perfection of the layers is very sensitive to growth parameters,⁵ such as growth temperature and As/Ga ratio used for the growth [often called the As/Ga beam equivalent pressure (BEP)]. Some discrepancy in the substrate temperature measurement is generally observed in different laboratories; therefore the same nominal growth temperature can in reality mean $\pm 30\text{-}50^\circ\text{C}$ difference. From our own investigations of many samples from different laboratories, the ones that were In bonded to a molybdenum block during growth show the most repeatable results.

Generally, samples grown at 200°C or higher on In bonded molybdenum blocks with a BEP of 10 and a growth rate of 1 $\mu\text{m/h}$ show high crystalline perfection up to 3 μm layer thickness. With increasing sample thickness, specific defects, called "pyramidal defects" can be formed. These pyramidal defects were described^{5,6} as defects with a well established core from which other defects, such as secondary microtwins, stacking faults, or dislocations, were formed. The thickness of the perfect material decreased drastically with decreasing growth temperature. At the same time, an increase of As concentration is observed in these layers. This increase in As concentration results in the expansion of the lattice parameter of the layer. The dependence of the lattice parameter change on excess As is shown in Fig. 1.

The crystal quality of the GaAs LT layers is very sensitive to any change in the growth temperature. For example a 5°C change makes a noticeable change in crystal quality: an increased density of pyramidal defects due to a decrease of the growth temperature are detected (Fig. 2).

Formation of pyramidal defects must be triggered at specific growth conditions. When the growth temperature is further decreased, the columnar growth of pyramidal defects is observed. This columnar growth is easy to observe at 180°C for the samples grown with a BEP of 10. In these samples, a change of the growth direction from [001] to [011] was observed. The appearance of pyramidal defects can be noticed at the periphery of the wafer even when the central part of the wafer shows crystalline perfection. Some changes in the temperature distribution across the wafer are expected despite the sample rotation during the growth. The LT layer thickness at which the start to appear decreases with decreasing growth temperature. Such changes are very difficult to detect with

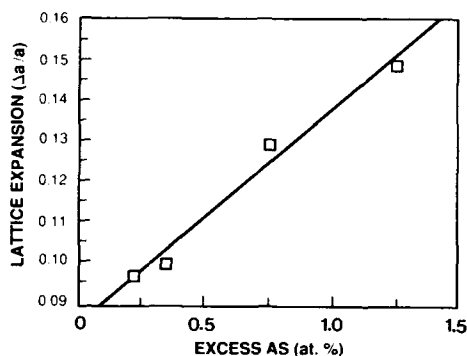


Fig.1. Dependence of the lattice parameter expansion of the LT-GaAs epilayers grown at 210, 200, 190, and 180°C on the excess As content in the layer.

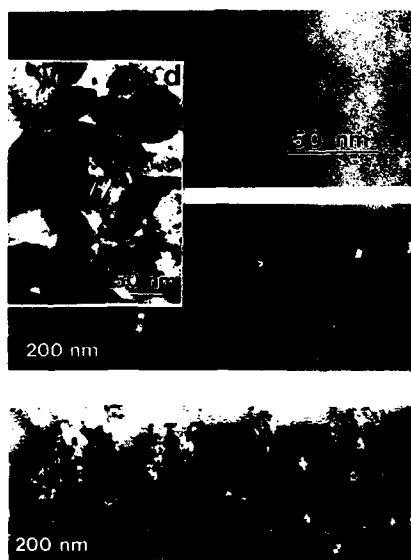


Fig.2. Plan-view micrographs showing distribution of pyramidal defects on the surface of 2 μm thick layer grown at: a) 200°C - no pyramidal defects; b) 195°C - some defects are already formed; c) 190°C - high density of defects, and d) 180°C - polycrystalline layer.

RHEED patterns. The details describing the correlation between crystalline perfection and the features of RHEED patterns will be described separately.⁷

If the LT layer is grown with a greater BEP than 10, different temperature is required to obtain monocrystalline material.^{8,9} Usually, for increased BEP, a higher growth temperature is required to obtain the same thickness of monocrystalline layer obtained for a BEP of 10. For a 1- μm layer thickness, the dependence on increasing in BEP is shown in Fig. 3a. Fig. 3b shows the dependence of monocrystalline layer thickness on growth temperature for a BEP of 20. Generally the layer grown with the higher BEP can be divided into three sublayers: the monocrystalline

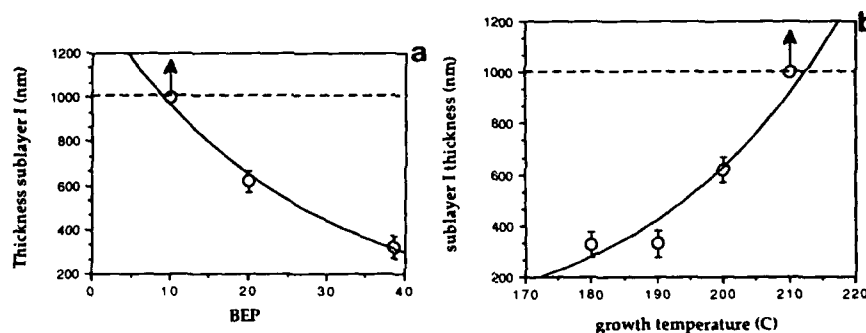


Fig. 3. a) Thickness of the defect-free layer as a function of BEP for a growth temperature of 200°C; b) Thickness of the defect-free layer as a function of growth temperature for a constant BEP of 20.

sublayer, the sublayer, with dislocations and stacking faults which are believed to be the origin of pyramidal defects, and the third part, a polycrystalline sublayer. At a particular monocrystalline layer thickness related to both the growth temperature and the BEP ratio, dislocations and stacking faults begin to form. With an increase in layer thickness, microtwins are formed. In these areas void formation was often observed. If the cap layer is grown on top of such a layer microtwins propagate through the cap layer, and the surface of the cap layer is usually undulated.

LAYERS GROWN BY GAS SOURCE MBE

The quality of the layers grown by gas source MBE is comparable to that of layers grown by solid-source MBE using As_2 . However, it appears that a very limited window in growth condition is required to obtain monocrystalline growth.¹⁰ One micrometer of monocrystalline layer thickness was obtained at 240°C at a V/III ratio of 35. At either a decreased or increased ratio, much smaller monocrystalline layer thickness can be obtained. The values of monocrystalline layer thickness obtained for different V/III ratios are shown in Table I. The layer quality and defect distribution reminds one of the layers grown by MBE at higher As/Ga BEP ratios.

The layers grown with higher BEP or grown by gas MBE using As_2 do not always form pyramidal defects, with well established cores, stacking faults, and microtwins originating from this core. However, the pyramidal defects that occurs in both growth modes can be formed even at the nominally same growth conditions. It is believed that conditions for twinning, which are main defects of pyramidal cores, determine the formation of these defects.

Table 1
Dependence of the monocrystalline layer thickness ($t_{\text{cryst.}}$) on growth conditions for gas MBE

Spec #	Species	LT thick. (μm)	$t_{\text{cryst.}}$ (μm)	T_g $^{\circ}\text{C}$	V/III ratio	t_{cap} (μm)
118	As_4	1	1	240	10	0.2
10	As_2	0.8	0.8	240	35	0.3
12	As_2	0.73	1	240	35	0.6
62	As_2	0.65	1	240	35	-
11	As_2	0.15	1	240	29	0.6
14	As_2	0.25	1	240	51	0.2

MODELS EXPLAINING THE BREAKDOWN IN CRYSTALLINITY OF THE LT-LAYERS

There can be several reasons for the breakdown of crystallinity of these layers. Eaglesham et al.¹¹ showed that a transition from the crystalline to the amorphous stage can be observed in Si and GaAs samples grown at low temperatures. Roughening of the growth surface was claimed to be responsible for breakdown of crystallinity in these layers. Only a particular single crystal layer thickness called h_{cpi} , dependent on growth temperature and growth rate, was observed. This observation is not surprising, since the surface diffusion at such low temperatures is very slow. At temperatures as low as 210°C, an abrupt change in the h_{cpi} layer thickness was observed (from 30 nm to 500 nm). This temperature of 210°C measured by Eaglesham¹¹ probably is similar to 180°C described in our work,⁶ since in our own experiments the transition to the amorphous stage was never observed.

A second reason for the breakdown of crystallinity may be strain buildup in the layer due to a specific excess of As responsible for the expansion of the lattice parameter. Based on this assumption, only a specific layer thickness, called the "critical layer thickness (h_c)," can be grown at a given growth condition. Upon exceeding this critical layer thickness, at normal growth temperatures misfit dislocations are formed at the surface which glide to the interface, relieving the misfit strain. However, at the low growth temperatures used here dislocation motion is very slow. Therefore, the strain energy cannot be relieved by misfit dislocation formation, and results in formation of misoriented GaAs nuclei that lead to polycrystalline growth. Evidence for this mechanism include dislocations and stacking faults found near the top of the crystalline layer (at the origin of pyramidal cores) that were obviously unable to glide down to the strained interface. The LT GaAs epilayer thicknesses at which the onset of pyramidal defects occur lie between the theoretical critical layer thickness (h_c) for pseudomorphic growth predicted by People and Bean¹² and by Matthews and Blakeslee.¹³ Thus it is possible that the elastic strain incorporated in the LT GaAs layers as a result of the excess As is responsible for the defects formed in the layer.

The third reason for the breakdown of crystallinity may be strain-induced As agglomeration.⁶ It is possible that only a specific amount of As can be accepted, and gives rise to the expansion of the GaAs lattice parameter. Any further excess of As must agglomerate on the surface of the GaAs layer. The As microclusters could initiate the growth of LT GaAs misoriented from the [001] direction and thus lead to the breakdown of crystallinity.

These last two mechanisms best explain our own observations. The presence of strain in as-grown layers has been confirmed by large-angle and classical convergent-beam studies. The largest strain was observed close to the interface with a buffer layer grown at 600°C. The convergent-beam pattern is not cubic in this part of the layer, while the top layer is fully cubic. However, the top layer has a different lattice parameter than the one observed in the substrate.

The expansion of the lattice parameter confirms earlier x-ray studies.³⁻⁶ Large-angle convergent beam patterns confirm this observation as well,¹⁴ and in addition provide information about different lattice parameters in the areas close to the interface and close to the surface. Since misfit dislocations were not observed in these parts of the layer, relaxation along the *c* axis (the growth axis) can be considered. The same change in lattice parameter close to the interface and at the top of the layer was independently observed by Kowalski et al by x-ray studies.¹⁵

Agglomeration of As can be easily detected in plan-view micrographs at the core of pyramidal defects.⁶ This means that As grains can be easily found on the top of the growth surface. Diffraction patterns confirming the existence of As grains on the top of the LT layers are shown in Fig. 4a. In addition, As agglomerates at the grain boundaries of the pyramidal core.

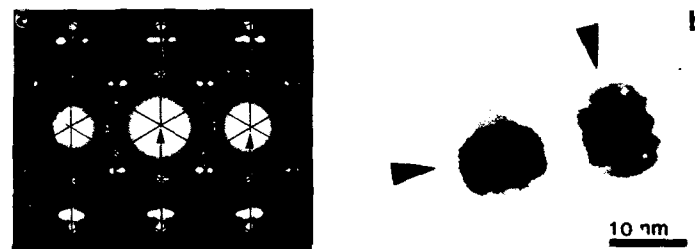


Fig. 4.a) Diffraction pattern of (0001) As taken from the top of pyramidal defect in plan-view sample; b) Moiré fringes on two precipitates showing rectangular patterns indicating strain relaxation on perpendicular direction for each precipitate.

ANNEALED LAYERS

Annealing of the layers either due to the growth of the cap layer on the top of the LT layer or due to annealing at As overpressure at 580°C or higher leads to the formation of As precipitates.^{6,16-18} Formation of these precipitates is always connected with a decrease in the lattice parameter to the substrate value. Formation of As precipitates leads to the relaxation of the stress in the material. This can be easily recognized from the moiré fringes formed on such precipitates visible in plan-view micrographs, which are very sensitive to the strain (Fig. 4b). It has been found that the strain within the precipitate is strongly anisotropic, leading to a lattice spacing compression in some directions and expansion in other directions. The moiré fringes do not form square figures, as would be required from two identical lattice spacings in the precipitate and in the matrix such as (220) and (-220). The observed moiré patterns are rectangular and perpendicular to each other on two adjacent precipitates (Fig. 4b). This suggests that as soon as one precipitate is formed to relax the strain in one crystallographic direction (semicoherent precipitate), immediately the other precipitate is formed to relax the stress in the perpendicular direction. Such an arrangement of precipitates leads almost to complete strain relaxation in the annealed layers.

The size of these precipitates and their distribution appear to be related to the growth parameters and annealing treatment. However, it is not very clear which growth parameters influence the original size of As precipitates in the monocrystalline part of the layer. For nominally similar growth parameters and annealing conditions, different sizes of As precipitates can be observed,¹⁸ and it is believed that the As/Ga ratio used during the growth can influence such behavior. For monocrystalline 2-μm-thick layers grown at 200°C with a BEP of 10, where conglomeration of As was not observed in as-grown layers, only small (2-4 nm in diameter), uniformly distributed As precipitates formed after annealing for 10 min at 600°C in As.

overpressure (Fig. 5a). In plan-view samples these As precipitates appear as semi-cubic and give rise to the extra spots very close to $\langle 220 \rangle$ matrix reflections (Fig. 5b). If a $3m$ orientation relationship typical for semicoherent "hexagonal" precipitates is calculated for the $[001]$ direction, similar extra spots close to $\langle 220 \rangle$ matrix spots form. Therefore, it is rather believed that small precipitates can be as well hexagonal precipitates. However, one feature in the diffraction pattern differentiates these small precipitates (2-4 nm) from the large ones (~10 nm): diffuse scattering close to $\langle 200 \rangle$ matrix reflections. This feature does not exist for larger precipitates. The position of these diffused scattered reflections changes with specimen tilt, and therefore, they can be considered as shape factor features for small precipitates. Theoretical calculations are in progress to confirm this assumption.

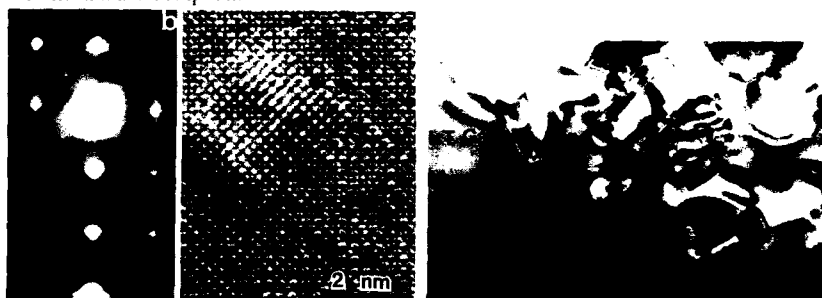


Fig. 5 a) A small precipitate in (001) projection which appear as "semi-cubic." Calculation of the diffraction pattern gives agreement for semicoherent hexagonal precipitates with $3m$ orientation relationship. Note an inelastically scattered reflections located near $\langle 200 \rangle$ matrix reflections shown in b) characteristic only for these small precipitates.

Fig. 6. Cross-section micrograph showing distribution of As precipitates and their increased diameter for the layer thickness where structural defects start to form.

For samples grown at lower temperatures with a BEP of 10, where pyramidal defects are formed, the same small precipitates are formed in the monocrystalline part of the layer, and much larger precipitates form in the vicinity of other defects. The annealing does not change the arrangement of existing structural defects, but they are good passes for As diffusion.

For samples grown with a higher As/Ga BEP ratio, if a cap layer was grown on top of the LT layer, As precipitates were formed in all three parts of the layer. In the monocrystalline part of the layer, As precipitates with a diameter much larger than those equivalent observed for a BEP of 10 were found. A slight increase in their diameter was observed with increased layer thickness, suggesting an increase of As concentration in the upper part of the layer. The larger precipitate size can be related to the fact that a noticeable size of As agglomeration (~0.5 nm) was already noticed for the as-grown layer grown with a As/Ga BEP ratio of 40. This was never observed for the layers grown with a BEP of 10, at for which it is believed that all As is dispersed. The precipitates formed in the vicinity of structural defects show drastic increase in size (see Fig. 6).

In the layers grown by gas source MBE using As_2 the growth of the cap layer leads to the formation of As precipitates. Their size and distribution is similar to the ones described above grown with a higher BEP.

Identification of As precipitates come from both diffraction patterns obtained from samples with precipitate sizes close to 10 nm and high-resolution imaging.^{6,19} High-resolution images especially in (110) projection (Fig. 9a) allowed us to determine that (0003) planes of As lie almost parallel to $\{111\}$ planes of GaAs, with $[-12-10]_p \parallel [011]_m$. The possible number of crystallographically equivalent variants of an orientation relationship, i.e., their multiplicity, was

determined from symmetry considerations. It was found out that $3m$ orientation relationship exists for these precipitates with four equivalent variants. This orientation relationship has the highest symmetry attainable by combining cubic matrix and hexagonal precipitate structures, and it provides the lowest interfacial and elastic energies. Only by taking into account all four variants of these precipitates can full agreement between an experimental and calculated diffraction pattern be obtained.

The knowledge of the orientation relationship is necessary to realize that imaging of the precipitates in the two-beam condition which is usually used for the determination of density of the precipitates in the LT layer²⁰ makes only a fraction of these precipitates visible. This was already shown in our previous paper¹⁸ where two perpendicular two-beam conditions were applied, for imaging of the same area of the sample containing precipitates and completely different precipitates give rise to the contrast in this two-imaging conditions. Therefore, determination of the density of precipitates based on such imaging conditions can lead to substantial mistakes.

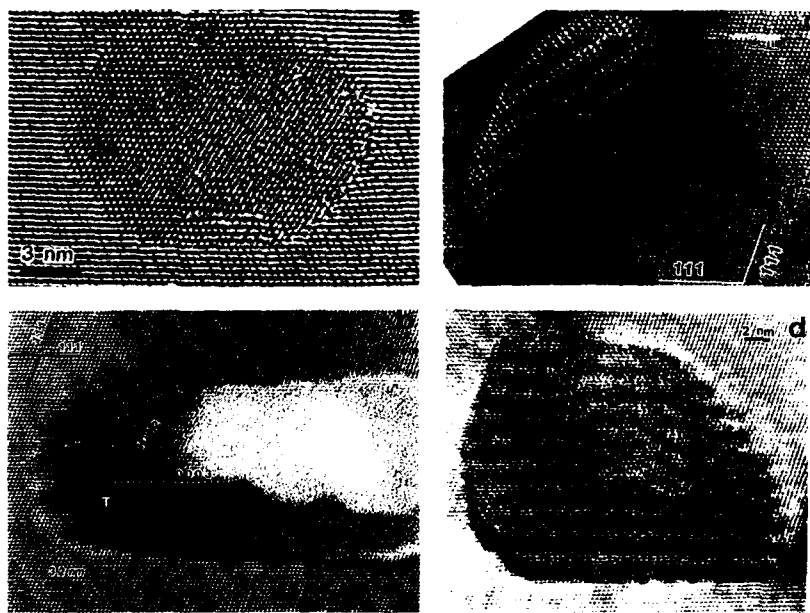


Fig. 7. Arsenic precipitates with their different orientation relationship: a) $3m$, b) twin- $3m$; c) $2nm$; and d) m .

Besides these precipitates with $3m$ orientation relationship of low formation energy more complicated precipitates were observed. Twinning within the precipitates can often be observed (Fig. 7b). The twin formation does not change the observed $3m$ orientation relationship; however, their energy formation can be slightly larger than for the simple $3m$ orientation. Twin formation in a hexagonal structure is rarely allowed, since twinning would not change the hexagonal arrangement of the planes. Therefore, one needs to remember that As has rhombohedral structure, where twinning is allowed, and only for simplicity can it be *causa* hexagonal. Such twinned precipitates were often found in the vicinity of other defects or in the monocrystalline part of the LT layer, which had precipitate diameters at least 10 nm or larger.

Therefore, it is believed that some conglomeration of As existed in as-grown layers in these parts of the material, which contributed to the local strain (or local strain from the defect), leading to higher-formation-energy precipitates in annealed samples.

Formation of precipitates with higher formation energy for samples grown with As/Ga BEP ratios of 10, was observed in the part of the layers with defects such as dislocations and stacking faults.^{6,17} Especially in those layers grown either with higher BEP or grown by gas source MBE, $2mm$ (Fig. 7c) or m (Fig. 7d) orientation relationships were observed even in the monocrystalline parts of the layers, where generally a much larger precipitate size was observed compared to these layers grown with a BEP of 10. Six variants of the precipitates with the $2mm$ orientation relationship and 12 variants of the precipitates with m orientation was determined.^{8,9}

Since the higher formation energy is required for the formation of such precipitates, it is believed that the local crystal arrangement, most possibly influenced either by local strain or agglomeration of As in as-grown layers, may be responsible for the formation of these high-formation-energy precipitates. It appears that annealing alone does not lead to the formation of precipitates with higher formation energy. This hypothesis were confirmed by isochronal annealing.

Isochronal annealing of the layers grown at 200°C with a BEP of 20 results in a drastic increase in precipitate size, with a substantial faceting of these precipitates (Fig. 8). Only small precipitates (~5nm in diameter) were observed in the first stage of annealing due to the growth of the cap layer at 580°C (Fig. 10a). This sample was cut into pieces and each piece annealed for 20 min at 750°C, 850°C, and 950°C. Faceting and increased precipitate size (Fig. 8 b,c,d) was the result of annealing. Their crystallographic configuration did not change due to annealing. Formation of faceted precipitates in the monocrystalline part of the layer is a direct result of annealing from the small precipitates uniformly distributed within the layer. The orientation relationship with the matrix remains $3m$. This allows us to conclude that local crystal arrangement influenced by strain must be responsible for the formation of precipitates with higher formation energy.

Due to annealing at higher temperatures, outdiffusion of As in both directions, i.e. to the surface and to the substrate, was noticed. This outdiffusion of As through the cap layer to the surface lead to the loss of material; as a result a very undulated surface was established. Deep diffusion in the direction of the substrate leads to the formation of As precipitates about 0.3 μ m below the original interface. This observation show that in order to keep constant concentration of As precipitates in the LT-layer or to avoid As doping of the layers adjacent to the LT layer some diffusion barriers need to be introduced. Three distinct rows of the large precipitates formed within the original LT layer. This arrangement of As precipitates reminds us very much of the distribution of As precipitates in AlAs/GaAs quantum wells;²⁰ however, in our case, AlAs layers were not introduced. Formation of these rows is most probably influenced by the diffusion length of As within LT GaAs layer.

TERNARY COMPOUNDS GROWN AT LOW TEMPERATURES

The structural quality of ternary compounds, such as InAlAs grown at low temperatures reminds us very much of the structure of LT GaAs and are described in detail in this volume.^{21,22} The layers grown at the lowest temperatures (~150°C) have a high density of pyramidal defects. However, at a specific growth temperature, a CuPt type of ordering on (111) planes can be detected in these layers, resulting in a special arrangement of diffuse scattering. This diffuse scattering can be explained due to the formation of very small domains. However, annealing of these layers does not lead to the formation of As precipitates, as was observed in the GaAs LT layers.

THE ROLE OF As PRECIPITATES IN THE ELECTRONIC PROPERTIES OF LT LAYERS

An absence of As precipitates in annealed LT-InAlAs layers is very important in order to understand the role of As precipitates in the electronic properties of all LT layers. It has been suggested that metallic As precipitates might form "buried Schottky barriers" with carrier-depletion regions around them.²³ For high precipitate density, these depleted regions would overlap and lead to the isolation properties of these layers. On the other hand, temperature-dependent conductivity measurements indicate that the electronic properties of both semi-insulating GaAs and LT-GaAs are controlled by mid-gap EL2-like defects, which are believed to

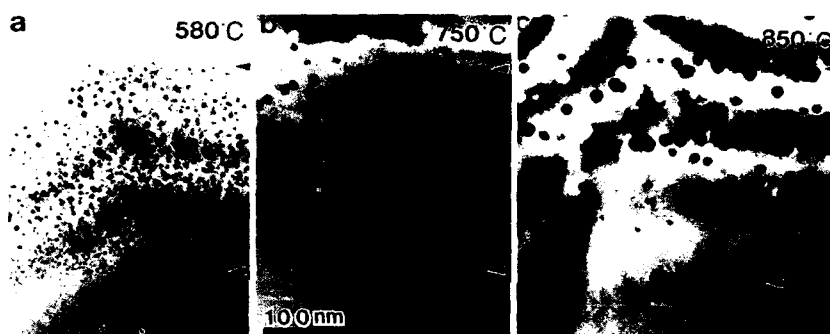


Fig. 8. Isochronal annealing of the LT-GaAs layer grown at 210°C with BEP of 20: a) growth of cap layer causing formation of uniformly distributed As precipitates; the lower and upper interface with LT-layer is marked; b) sample shown in 'a' annealed for 20 min at 750°C in As overpressure; c) sample shown in 'a' annealed for 20 min at 850°C in As overpressure; d) sample shown in 'a' annealed for 20 min at 950°C in As overpressure. Note As outdiffusion and surface undulation with increasing temperature.



be As-antisite defects.²⁴⁻²⁶ The observations made here for LT-GaAs are consistent with either model. However, the fact that As precipitates are not formed in the annealed, semi-insulating LT-InAlAs layers suggests that deep-level defects might play an important role in understanding of semi-insulating behavior of LT layers.

Another important problem is to understand the role of defects on the lifetime of minority carriers in the LT layers. There are some reports that the lifetime can be as short as 200 fsec, but there is no systematic study to determine if As precipitates make this lifetime so short or if pyramidal defects can play an important role as well. A few of our own observations show that the shortest reported life times are for samples where pyramidal defects are present.²⁷ This observation is not surprising, since carrier recombination on structural defects such as dislocations, stacking faults, and microtwins is well known. However, our recent observations show that very short lifetime, (600 fsec) can be obtained for samples without pyramidal defects.²⁸ The 1- μm -thick sample had uniformly distributed precipitates with an average diameter of 9 nm and a density of $\sim 3 \times 10^{15} \text{ cm}^{-3}$. For a sample with approximately the same diameter but with a 0.5- μm top layer and a density of precipitates three times higher the lifetime increased more than one order of magnitude. However, this sample had a LT-sublayer adjacent to the substrate with an extremely low density of precipitates, and it is not clear how to combine the role of these two sublayers in order to understand the precipitate influence on the carrier lifetime. If only the same top sublayers are considered in both samples, one would conclude that a higher density of precipitates elongates the lifetime of minority carriers. This would mean that very distinct density of precipitates is required to obtain the shortest possible lifetime or that other mechanism is playing an important role. Further study is necessary in order to understand the role of precipitates and the role of point defects in this material.

CONCLUSIONS

The structure of LT-GaAs layers was described. It was shown that the structural quality of the layers is very sensitive to growth parameters, such as growth temperature and As/Ga beam equivalent pressure used for the growth. For a BEP of 10 and a growth rate of 1 $\mu\text{m}/\text{h}$, high monocrystalline perfection of the layer can be obtained for growth at 200°C and layer thicknesses up to 3 μm . Breakdown of crystallinity is observed for the layer thickness above 3 μm . So-called pyramidal defects are formed in the subsurface areas. Similar defects are formed if this growth temperature decreases. At lower growth temperatures higher As concentrations can be incorporated, and only a smaller layer thickness of high crystalline perfection can be grown. At even lower growth temperatures, the layer is polycrystalline, with As segregated at the grain boundaries. The as-grown layers are strained, and the strain was considered as one reason for the breakdown of crystallinity of these layers. Some other reasons for the breakdown of crystallinity were discussed as well.

For layers grown at higher As/Ga BEP ratios a higher growth temperature is required to obtain similar crystalline perfection.

The quality of the layers grown with gas MBE using As_2 is very similar to those obtained with As_4 ; however, it appears that a very specific As/Ga ratio must be applied in order to maintain the high crystalline quality. For higher and lower ratio the monocrystalline layer thickness decreases dramatically.

The semi-insulating properties of these materials are observed only after annealing. The annealing is generally part of the subsequent growth of a device structure at 580-600°C on top of the LT-GaAs layers. The annealed layers show a decrease in lattice parameter compared to that of the substrate, a change accompanied by the formation of a high density of small As precipitates. These precipitates are semi-coherent, and they are of the lowest formation energy that exists to accommodate hexagonal and cubic structure together. The formation of these As precipitates is connected with the strain relaxation in these layers. These kinds of precipitates are formed in the monocrystalline parts of the LT-layers grown with low As/Ga BEP ratios. If a higher BEP ratio is

used, a more metastable configuration of these precipitates forms, which requires higher formation energies. Similarly, high-formation-energy precipitates are formed in the vicinity of structural defects even in the annealed layers grown with BEP ratios of 10. Therefore, it is believed that the local crystal strain influences the formation of the precipitates with higher formation energy. The role of As precipitates in the electronic properties of these layers is not fully understood; however, an interesting model that suggests carrier depletion around them ("the buried Schottky barrier model") was proposed as explanation of the semi-insulating properties of these materials.²³

In the present work it was shown that short lifetime (600 fsec) of minority carriers can be obtained in monocrystalline LT-GaAs layers with a high density of As precipitates.²⁸ Further studies are needed to distinguish between the role of point defects and As precipitates in these layers.

The growth of ternary compounds (InAlAs) at low temperature appears more complex, but at a specific growth temperature an ordering on (111) planes can be formed. Such ordering can decrease minority carrier scattering and can change the band structure of the material; therefore, interesting applications can be considered for these layers. These layers differ from LT-GaAs after annealing, since As precipitates were not observed after annealing. In this way "the buried Schottky barrier" model can be tested as a general model for understanding semi-insulating behavior of LT layers. Two competing models used: "the buried Schottky barrier" model²³ and the model with deep level point defects,²⁴⁻²⁶ to understand semi-insulating properties of LT-GaAs layers cannot be rejected at the moment but only the second model can be applied to LT-InAlAs layers.

ACKNOWLEDGMENTS

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INCORPORATION OF EXCESS ARSENIC IN GaAs AND AlGaAs EPILAYERS GROWN AT LOW SUBSTRATE TEMPERATURES BY MOLECULAR BEAM EPITAXY

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ABSTRACT

Excess arsenic can be incorporated in GaAs and AlGaAs epilayers by growing at low substrate temperatures (LT-GaAs and LT-AlGaAs) by molecular beam epitaxy (MBE). Upon annealing these epilayers, the excess As precipitates forming GaAs:As and AlGaAs:As. Using transmission electron microscopy (TEM), we have measured the densities and sizes of the As precipitates and thereby determined the amount of excess As incorporated in these epilayers. The volume fraction of excess As as a function of inverse substrate growth temperature follows an Arrhenius-type behavior with an activation energy of 0.87 eV. The sizes of the As precipitates increase and the densities decrease with increase anneal temperatures; for Si-doped GaAs:As this results in n-type material when the densities become small enough that the depletion regions around the As precipitates no longer overlap. Also investigated is the formation of As precipitates at GaAs/AlGaAs heterojunctions and superlattices, and our attempts to tailor the As precipitate distribution.

INTRODUCTION

Typical MBE of GaAs is at substrate temperatures of about 600°C. At this substrate temperature, for high quality stoichiometric films an As₄/Ga flux of somewhat greater than 10 is necessary [1]. If one maintains such an excess flux of As but reduces the substrate temperature to 200-250°C, as much as 1% excess As can be incorporated into the film [2]. This excess As is incorporated in the form of As anti-sites and interstitials; the interstitial As results in an increase in the lattice constant of the film [2-5]. Upon annealing this highly non-stoichiometric material at temperatures of 600°C, the lattice constant approaches that of highly stoichiometric GaAs [2-5]. Furthermore, as determined by electron paramagnetic resonance, the amount of As anti-site defects falls below the detectability limit after such anneals [2,6]. Original TEM studies of such annealed films indicated no difference in contrast between the substrate and epilayer, similar dislocation densities, and no additional defects [2,6]! This was indeed a puzzle because where had all the excess As gone? When we performed TEM studies of our GaAs films that had been grown at 250°C we found that upon annealing at 600°C our excess As was forming precipitates with an average diameter of 50 Å and a density of $1 \times 10^{17} \text{ cm}^{-3}$. This is what happens to the excess As in all such annealed material [7-10] including AlGaAs [11]. Also, very similar behavior is observed both structurally [12] and electronically [13] if the dimer species As₂ is used for MBE instead of the tetramer As₄.

Having such a large concentration of As precipitates in a GaAs matrix (GaAs:As) has to play an important role in the electrical [14] and optical properties [15,16] of GaAs:As. Therefore the factors controlling the final sizes and distributions of the precipitates are important. In this paper we investigate how the substrate temperature affects the incorporation of the excess As in GaAs and AlGaAs and how the anneal conditions affect the formation of the As precipitates. We also look at the formation of precipitates at AlGaAs/GaAs heterojunctions and superlattices, and methods to control the distribution of As precipitates.

TYPICAL FILM GROWTH AND ANNEAL PROCEDURES

The films used in this work were grown in Varian GEN II MBE systems on two-inch diameter substrates. Growth rates were typically $1 \mu\text{m/h}$ for both AlGaAs and GaAs layers. This was accomplished for AlGaAs/GaAs heterojunctions and superlattices by the use of two Ga effusion furnaces. Films were grown using either the dimer As_2 or the tetramer As_4 with similar results except the incorporation of the As is more efficient when using As_2 [12]. Typical group V to group III beam equivalent pressures used were 20, as measured with an ion gauge in the substrate growth position. Film growth started with a GaAs buffer layer grown at a substrate temperature of 600°C . The buffer layers typically ranged in thickness from $0.5 \mu\text{m}$ to $1.0 \mu\text{m}$. After growing the buffer layer, the substrate temperature was reduced to 200 to 250°C while continuing to grow GaAs. This results in a $0.25 \mu\text{m}$ temperature transition region. After film growth at low substrate temperatures, different methods were used for annealing. One anneal procedure was in the MBE system under the group V flux at a temperature of 600°C for 1h. The other method used for annealing was in a rapid thermal annealer (RTA). The RTAs ranged in temperature from 600°C to 900°C for 30 s.

SUBSTRATE TEMPERATURE DEPENDENCE OF ARSENIC INCORPORATION

As might be expected, the incorporation of excess As is a strong function of the substrate temperature during MBE [11]. To investigate this substrate temperature dependence of incorporation of excess As, the following experiment was performed. After lowering the substrate temperature to 225°C , $0.25 \mu\text{m}$ of LT-GaAs was grown, then the substrate temperature was quickly ramped by 25°C . This temperature ramping occurred in about one minute corresponding to growth of about 150 \AA . After growing another $0.25 \mu\text{m}$ of LT-GaAs at 250°C , the substrate temperature was again ramped by 25°C . This process was continued till a $0.25 \mu\text{m}$ LT-GaAs layer was grown at a substrate temperature of 350°C . The substrate temperature was then ramped to 600°C , the growth terminated, and the sample annealed for 1h.

The results of the TEM analysis of this film are shown in Table I, Fig. 1, and Fig. 2. As the substrate temperature is increased, there is a decrease in the density and diameter of the As precipitates. Furthermore, the plot of the natural logarithm of the relative volume fraction of As precipitates versus the inverse of the substrate growth temperature in Fig. 1 indicates an Arrhenius-type relationship corresponding to an activation energy of 0.87 eV [12]. A typical distribution of As precipitate sizes is shown in Fig. 2 for the $0.25 \mu\text{m}$ portion of the film that was grown at a substrate temperature of 250°C .

Table I. Relative arsenic precipitate density and average diameter as a function of substrate growth temperature, and the corresponding relative volume fraction of arsenic in precipitates. The densities and therefore the volume fractions are relative values because only a portion of the arsenic precipitates was included in the measurements.

Temperature (°C)	Relative density ($\times 10^{16} \text{ cm}^{-3}$)	Diameter (Å)	Relative volume fraction ($\times 10^{-3}$)
225	4.3	74	3.410
250	3.9	55	0.951
275	1.7	61	0.635
300	0.78	76	0.556
325	0.52	46	0.077
350	0.39	29	0.016

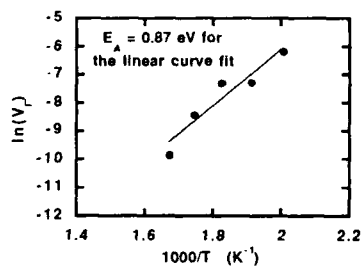


Fig. 1 Relative arsenic precipitate volume fraction as a function of inverse substrate growth temperature.

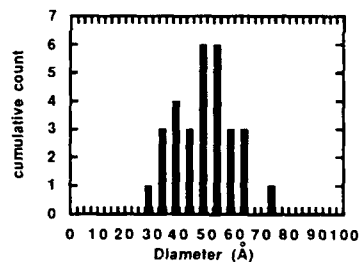


Fig. 2 Size distribution of As precipitates for the layer grown at a substrate temperature of 250°C and annealed for 1 h at 600°C.

EFFECT OF ANNEAL ON PRECIPITATE FORMATION

The effects of temperature of anneal on the formation of As precipitates was investigated using rapid thermal anneals (RTA). The film used was a Si-doped LT-GaAs layer grown at a substrate temperature of 250°C; the Si concentration was $5 \times 10^{18} \text{ cm}^{-3}$. Only the LT-GaAs was doped and the sample was grown on a semi-insulating substrate so that the electrical properties of the LT-GaAs could be monitored as a function of the anneals. The sample was then removed from the MBE system after growth of the LT-GaAs without any other high temperature steps. The sample was cleaved so that different anneals could be performed. RTAs were performed for 30 s; samples were annealed at temperatures of 700°C, 800°C, and 900°C.

Shown in Fig. 3 are the cross-sectional TEM images of the samples annealed at 700°C and 900°C. The samples were prepared by ion-milling and are wedge-shaped. Therefore the thickness contours seen in Fig. 3 resulted from the dynamical diffraction effect. The different spacings of the thickness contours in the two images are due to their different shapes and the fact that the extinction distance of 200 kV electrons in GaAs for the (111) reflection is 545 Å. As the anneal temperature increases, the average size of the precipitates increases while the density decreases. These results are summarized in Table II. For each anneal temperature, approximately the same volume fraction of As was obtained. Therefore even at the lowest temperature anneal, 30 s was long enough for the excess As to incorporate into precipitates. With higher anneal temperatures, the coarsening of the precipitates has proceeded further during the 30 s duration of our anneals. Furthermore, as the precipitate density decreases with increased anneal temperature, the films begin to exhibit n-type conductivity as determined by Hall measurements. This is a result of the depletion regions around the precipitates no longer overlapping as their density decreases. Our observations of the onset of n-type conductivity of Si-doped LT-GaAs with increase temperature of a RTA are similar to that previously reported by Schaff [17].

Table II. Effects of temperature of a 30 second rapid thermal anneal on As precipitate formation.

Anneal Temperature	Average precipitate diameter (Å)	Average inter-particle spacing (Å)	Precipitate Density ($\times 10^{16} \text{ cm}^{-3}$)	Precipitate Volume Fraction
700°C	70	225	8.7	0.015
800°C	150	475	0.93	0.016
900°C	200	675	0.325	0.013



Fig. 3a TEM image of an LT-GaAs sample which was annealed at 700°C for 30 s.



Fig. 3b TEM image of an LT-GaAs sample which was annealed at 900°C for 30 s.

PRECIPITATE FORMATION IN AlGaAs/GaAs STRUCTURES

Two structures grown to investigate the formation of precipitates in AlGaAs/GaAs structures are shown in Fig. 4a and 4b. The first one consisted of thick (0.2 μm) GaAs and AlGaAs regions so the formation of the precipitates at each heterojunction was not influenced by the other heterojunctions in the film. This structure is shown in Fig. 4a. The LT-GaAs and LT-AlGaAs regions were grown at a substrate temperature of 250°C and then the film was annealed in the MBE system for 1 h at 600°C. Three different $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterojunctions of aluminum mole fractions $x = 0.2, 0.3$, and 0.4 were contained in the film. The second film, shown in Fig. 4b, consisted of six ten-period $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ superlattices of varying well and barrier widths ranging from 25 Å to 200 Å. After removing this sample from the MBE system, a rapid thermal anneal at 700°C for 30 s was used to form the As precipitates.

At each $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ interface of the Fig. 4a film structure, a narrow precipitate depletion (PD) zone was found on the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ side [18]. Figure 5 is a 200 dark field image of an interface between $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and GaAs. In the image, $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and GaAs layers appear as bright and dark regions respectively, and the As precipitates are seen as dark spots. As seen in the image, a narrow PD zone with a width of about 250 Å exists along the interface on the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ side. The image also shows the existence of a precipitate accumulation (PA) zone on the GaAs side of the interface, in which the density of the As precipitates is higher than that in the interior of the GaAs layer. These PD and PA zones were observed at all $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ interfaces in this sample.

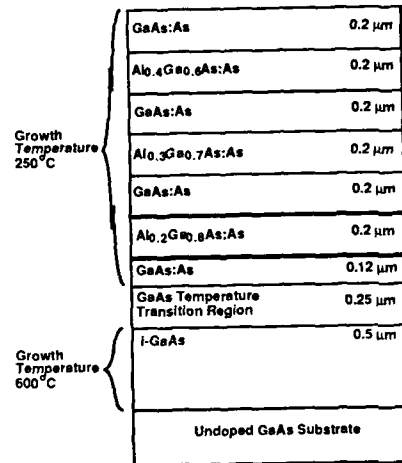


Fig. 4a Cross-section of the multiple heterojunction sample

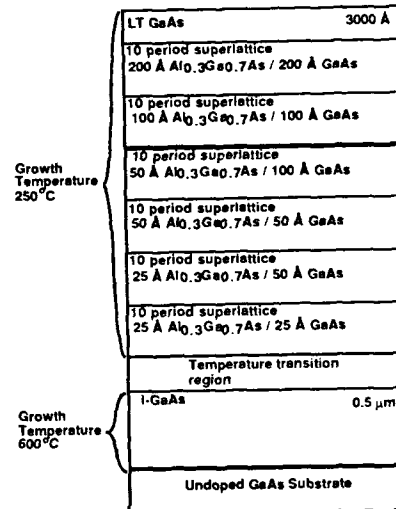


Fig. 4b Cross-section of the multiple superlattice sample

Fig. 5. 200 dark field image of an interface between LT-Al_{0.3}Ga_{0.7}As and LT-GaAs which was annealed to cause the excess As to precipitate.

Two important points regarding the PD and PA zones were observed. First is the existence of similar PD and PA zones in both normal and inverted interfaces, which indicates no significant dependence of the formation of these zones on the growth sequence. The second point is the nearly identical widths of the PD zones at all interfaces, suggesting no or a weak dependence of the excess As diffusivity on the Al concentration in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers.

TEM images of the Fig. 4b superlattice structure are shown in Figs. 6a and 6b, revealing several very interesting observations. For the superlattices with GaAs wells whose thickness is 100 Å or larger, the precipitates are constrained to the GaAs regions and do not extend into the AlGaAs regions. The shortest period superlattice, with 25 Å AlGaAs barriers and 25 Å GaAs wells, is almost completely free of precipitates; an increase in precipitate density is observed in the GaAs buffer layer below this superlattice and in the superlattice just above. Furthermore, for superlattices with GaAs wells of 50 Å widths, the As precipitates extend into the AlGaAs barriers.

The observations of precipitate formation at AlGaAs/GaAs heterojunctions and in superlattices can be explained if the interfacial energy of an As precipitate in contact with GaAs is smaller than for an As precipitate in contact with AlGaAs. Although experimental data is not available to support this suggestion, we believe that it is reasonable based on the fact that the bond energy of Al-As is higher (1 eV) than that of Ga-As (0.8 eV) [19]. The precipitate/matrix interfacial energy is known to have direct influence on the nucleation and coarsening stages of the precipitation process. According to theories of homogenous nucleation, the critical size for nucleation of precipitates is proportional to the interfacial energy of the precipitates/matrix. Therefore, the critical size for the formation of As precipitates in AlGaAs is larger than in GaAs. This implies that the incubation time is higher for nucleation of As precipitates in AlGaAs than in GaAs. There is a finite time during which the GaAs matrix is depleted of excess As atoms due to their precipitation, while the AlGaAs matrix still retains a large excess of As. Diffusion of the excess As in the AlGaAs matrix to the GaAs matrix would occur, resulting in a continued accumulation of As precipitates in the GaAs. In the coarsening stage, the distribution of precipitates changes through exchange of excess solute atoms among precipitates, driven by the tendency of the system to reduce its precipitate/matrix interfacial energy. In homogeneous systems, larger precipitates increase their sizes at the expense of smaller precipitates during this stage [20]. In AlGaAs/GaAs heterostructure systems, on the other hand, precipitates in GaAs layers grow at the expense of those in AlGaAs layers owing to the differences in precipitate/matrix interfacial energies, resulting in further development of PD and PA zones at heterojunctions. In superlattices, when the thickness of the GaAs layers is large enough to accommodate precipitates larger than the critical size, then the precipitates would be confined to the GaAs wells; precipitates with their boundaries close to the AlGaAs/GaAs interface would be constrained to grow within the GaAs wells, since their extension into the AlGaAs barriers would lead to an increase in the interfacial energy. Furthermore, the precipitation of As within thin GaAs wells is not energetically favorable since this would require a large density of precipitates with sizes less than the critical size and would lead to an increase in the interfacial energy of the system. Therefore when the GaAs well widths are less than the critical size of the precipitates, the precipitates will extend into the AlGaAs barriers unless the superlattice is short enough that the excess As can diffuse to regions of lower precipitate to matrix interfacial energies as seen in Fig. 6a.

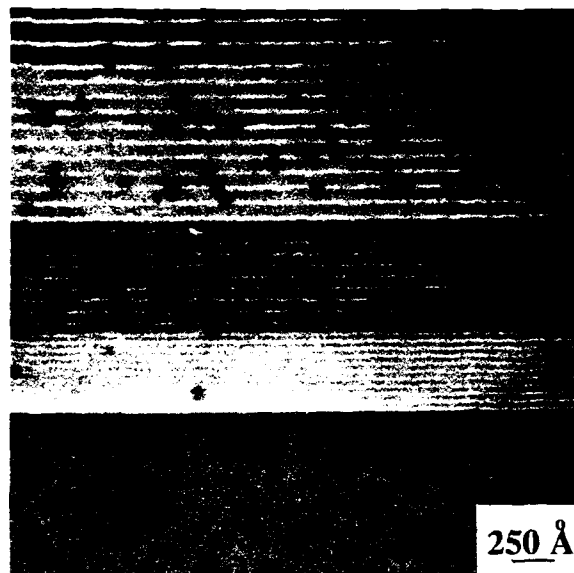


Fig. 6a TEM image of the lower superlattice sections of Fig. 4b.

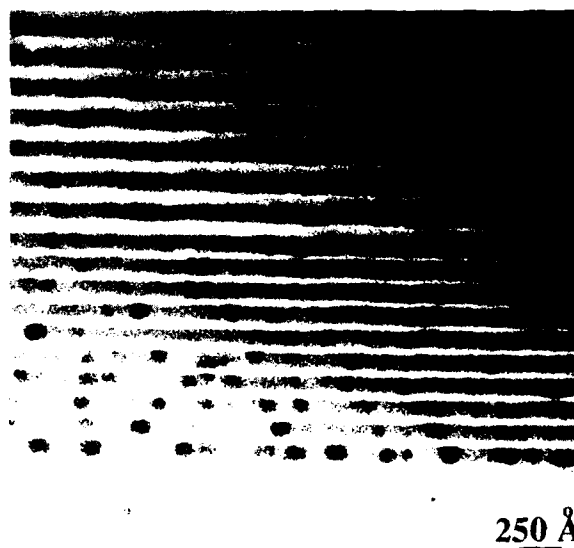


Fig. 6b TEM image of the upper superlattice sections of Fig. 4b.

CONTROL OF ARSENIC PRECIPITATE DISTRIBUTION

Since As precipitates play such an important role in the electrical and optical properties of GaAs:As, the ability to tailor their distributions would be very useful. It would be very important from a technology point of view to be able to fabricate films that had a very large sheet density of As precipitates or maybe even a continuous layer. This would result in a buried metallic-like As layer in a high quality GaAs matrix. The obvious applications would be for metal-based transistors, permeable base transistors, long-wavelength optical detectors, etc.

One method to obtain a high sheet density of As precipitates is to take advantage of the preferential formation of precipitates in GaAs regions compared to AlGaAs regions. Preliminary investigations into this method have been performed using GaAs quantum wells between thick AlGaAs barriers as shown in Fig. 7. This sample was not annealed in the MBE system but removed and cleaved so that different anneals could be performed to investigate the preferential formation of the As precipitates in the GaAs quantum wells. The TEM image for a sample that was annealed at 800°C for 30 seconds is shown in Fig. 8. Clearly seen is a large accumulation of As precipitates in the GaAs quantum wells and a very reduced precipitate concentration in the thick AlGaAs barriers.

Another method to enhance precipitate formation is to provide nucleation sites for the As precipitates. This could then result in a large precipitate concentration after precipitate growth and coarsening in the region of the nucleation sites. One method of providing such nucleation sites is with the incorporation of impurities such as a dopant. We have attempted this technique using a thin sheet of silicon embedded in a LT-GaAs layer. A cross-sectional TEM image of this structure is shown in Fig. 9. In the LT-GaAs region there is a clear enhancement in the precipitate concentration in a narrow band that corresponds to the region that was doped with silicon.

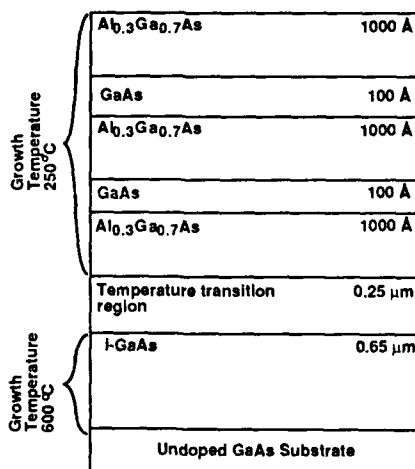


Fig. 7 Cross-section of film structure used to obtain high sheet concentrations of arsenic precipitates.



Fig. 8 TEM image of quantum well regions of Fig. 7.



Fig. 9 TEM image of an LT-GaAs layer that contains a region doped with Si. In the Si-doped region there is an enhancement in the As precipitate concentration.

SUMMARY

Excess As can be incorporated in GaAs and AlGaAs epilayers by growing at low substrate temperatures by molecular beam epitaxy. Upon annealing these epilayers, the excess As precipitates forming GaAs:As and AlGaAs:As. Using transmission electron microscopy, we have measured the density and sizes of the As precipitates and thereby determined the amount of excess As incorporated in these epilayers. The volume fraction of excess As as a function of inverse substrate temperature follows an Arrhenius-type behavior with an activation energy of 0.87 eV. The sizes of the As precipitates increase and the densities decrease with increase anneal temperature; for Si-doped GaAs:As this results in n-type material when the densities become small enough that the depletion regions around the As precipitates no longer overlap.

Also investigated was the formation of As precipitates at GaAs/AlGaAs heterojunctions and superlattices. At AlGaAs/GaAs heterojunctions there is a diffusion of excess As from the AlGaAs to the GaAs during anneals. This results in a precipitate free zone on the AlGaAs-side and a precipitate accumulation zone on the GaAs-side of the heterojunction. In AlGaAs/GaAs superlattices, when the critical size of the precipitates is less than the GaAs well width the precipitates are confined to the GaAs well regions. When the GaAs well widths are less than the critical size of the precipitates, the precipitates will extend into the AlGaAs barriers unless the superlattice is short enough that the excess As can diffuse to regions of lower precipitate to matrix interfacial energies. Using this diffusion of excess As from AlGaAs to GaAs, we have formed sheets of very high As precipitate densities by using GaAs quantum wells between thick AlGaAs barriers. As another attempt to tailor As precipitate distributions, we incorporated nucleation sites for the As precipitates. These nucleation sites were regions doped with silicon and resulted in greatly enhanced precipitate concentration in these regions.

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X-RAY DIFFRACTION STUDIES OF LOW TEMPERATURE GaAs

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ABSTRACT

GaAs layers grown by molecular beam epitaxy (MBE) at low substrate temperatures (LT GaAs) were studied in a novel purpose designed X-ray experiment. It combines X-ray double crystal rocking curve measurements with some elements usually found in optical setups like light illumination at liquid nitrogen temperatures applied to transfer EL2 type defects into metastable state. Ability to record such transfers with the X-ray experiment as well as large lattice relaxation accompanying this process is presented.

Introduction

The LT GaAs grown by molecular beam epitaxy at temperatures 190° to 300°C exhibit high resistivity thus making it perfect for other technological purposes like metal-semiconductor field-effect transistor (MESFETs) structures or high electron mobility transistors (HEMTs). The recent growth of interest in those materials is stimulated by still unresolved crystal structure as well as electronic properties. Some preliminary results concerning crystal structure are already available [e.g.1,2] and show first of all that the layers of LT GaAs are crystalline and [2] that there is a mismatch of the lattice constant between substrate and the layer. Lattice mismatch was established [2] to be about $\Delta a/a = 10^{-3}$ and was connected with the excess arsenic present in the layer. The mismatch can be eliminated by annealing the crystals above 600°C. One of the main structural properties of the LT GaAs is the presence of large amounts of excess (up to 1%) arsenic as recorded for example by auger electron spectroscopy [3]. EPR (electron paramagnetic resonance) studies [2] show that arsenic antisite As_{Ga} defects with the concentrations around 10^{20} cm^{-3} were detectable in as grown LT GaAs. The optical absorption measurements [4,5] confirmed some similarities between defects in LT GaAs and EL2 defects in semi-insulating (SI) melt grown GaAs e.g. comparable absorption spectra, metastability, thermal dependence of the centers recoverable from the metastable state at around 120 K. But there are significant differences between EL2 in SI GaAs (in both charged $EL2^+$ and neutral $EL2^0$ states) and EL2-like defects in LT GaAs [2,4,5] : i) EPR defect signal for LT GaAs is not optically quenchable, ii) maximal efficiency of the metastable transfer is wavelength dependent-900 nm for LT GaAs and 1050 nm for SI GaAs, iii) absorption spectrum of LT GaAs is not fully quenchable when transferring defects into metastable state, iii) recovery from the metastable state can be induced by light of the wavelength 1350 nm in LT GaAs but not in bulk SI GaAs.

Method

The X-ray double crystal spectrometer is already well established tool for studying thin semiconductor layers grown on thick substrates [e.g. 6,7,8]. The amount of information yielded from this type of measurements varies from composition studies and lattice mismatch measurements to layer thickness matching and confirmation of lattice perfection. We have combined this in a way standard technique with the conditions usually established for optical measurements of metastable behavior of EL2 type defects in melt grown GaAs. Our samples were measured at three stages : first at room temperatures then after cooling in darkness at 77 K and finally we measured them at 77 K after white or monochromatic light illumination. At all those stages we have taken repeated sets of "rocking curves" employing [400] Bragg reflection with $\text{CuK}\alpha_1$ radiation or [800] Bragg reflection with $\text{CuK}\beta_1$ radiation in so called (+,-) non dispersive mode. This type of X-ray setup with liquid nitrogen continuous-flow cryostat for sample cooling was recently successfully used for examination of EL2 defects in SI GaAs [9] as well as for DX centers in GaAlAs:Te [10] thus constituting a novel approach to metastability studies of point-like defects.

Results

Three as grown samples of LT GaAs grown by MBE at 190°C (1.5 μm), 220°C (2 μm) and 220°C (3.5 μm) on melt grown SI GaAs substrate were examined. From optical absorption measurements [4] concentration of EL2-like defects was established to be about 10^{20} cm^{-3} in those samples. Room temperature measurements (fig.1a, fig.2a) show two distinctive Bragg peaks one from

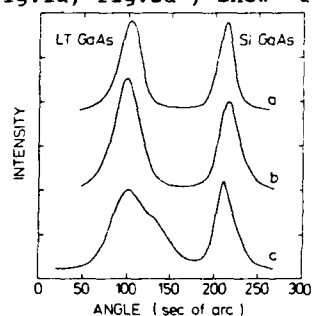


Fig.1 X-ray rocking curves for (400) $\text{CuK}\alpha_1$ reflection of LT GaAs layer on SI GaAs a) 295 K b) 77 K after cooling in darkness c) 77 K after cooling in darkness and 4 min. illumination with white light. Layer thickness $d=2 \mu\text{m}$.

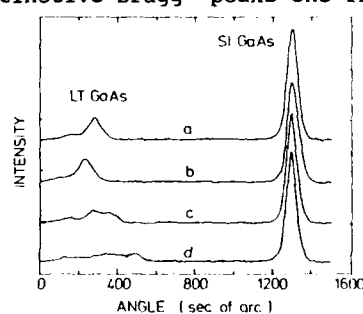


Fig.2 X-ray rocking curves for (800) $\text{CuK}\beta_1$ reflection of LT GaAs layer on SI GaAs a) 295 K b) 77 K after cooling in darkness c) 77 K after cooling in darkness and 5 min. illumination with 900 nm light d) 77 K after cooling in darkness and illumination with 900 nm light for 15 min. Same sample as in fig.1

LT GaAs layer and second from substrate thus showing that lattice parameter of the layer was markedly different from the substrate. Slight asymmetry on the left-hand side of the layer peak in fig.1a and more pronouncedly seen on fig.2a as a tail is a clear indication of a lattice parameter grading in the layer for the direction perpendicular to the layer surface. Very recently it was established [11] that for samples used in this work lattice constant perpendicular to the surface is graded with the higher values at the layer interface with the substrate, diminishing towards the free surface. As regards a component parallel to the interface it was concluded that lattice parameter is equal to the substrate value. All those measurements were done only for room temperatures. In fig.1b and fig.2b (after cooling in darkness) both peaks from the layer and from the substrate are slightly broadened. It is a indication of some lattice changes induced by cooling in darkness for samples reach in EL2 like defects. We have already observed such effects in SI GaAs [9] and to our knowledge it was never reported for those type of materials. Illumination with white light (fig1.c) or with wavelength 900 nm (fig.2c) at $T = 77$ K lead to a strong broadening of the layer peak to almost twice the initial full width at half maximum (FWHM) value and shift towards the substrate peak, which now was narrower then before the illumination. Behavior of the substrate peak is fully consistent with our previous [9] results for SI GaAs. Prolonged illumination with monochromatic light (fig.2d) caused further broadening and lowering of the layer peak. Total recovery of the layer peak could be obtained after warming the sample up to 140K. Moreover it was found that almost full recovery of the layer peak could be also obtained by illumination with light of wavelength 1350 nm. These results of the X-ray experiment were compared with the previous optical absorption measurements [4] and especially with temperature and illumination cycles of the near-infrared absorption band due to arsenic antisite defects. This allowed us to ascribe the changes of the LT GaAs lattice structure (as recorded by X-ray rocking curve) to the transformations of arsenic antisite defects from their normal to the metastable configuration.

DISCUSSION

Experimental rocking curves such as on fig.1 and fig.2 are usually used to gain information about the thin layers by direct comparison with computer calculated curves which are modelled by using X-ray dynamical theory [6,7,8]. Computer calculated curves were used in this work to get an information on lattice mismatch in the layers of LT GaAs taken through usual temperature and illumination cycles for studying metastable defects. Lattice mismatch profile as in fig.3 is used in computations as fitting parameter and best result is taken as final. In our case we possess some preliminary results as to the lattice mismatch profile in the layer [11] showing gradient of the lattice parameter across the layer. Starting from this point and employing required computer simulations involving convolution with the X-ray monochromator function we have been able to reproduce to very satisfactory level our experimental curves (fig.1, fig.2) It also appeared

to be necessary to introduce overall curvature of the samples induced by layer presence as it is frequently observed for such a structures. Main objective of our calculations e.g. lattice mismatch profile is summarized in fig.3. For room temperatures we have confirmed previous results [11] as to the presence of lattice parameter gradients spreading

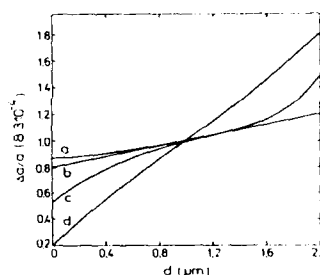


Fig.3 The mismatch of LT GaAs $[(a_{\text{LTGaAs}} - a_{\text{SIGaAs}})/a_{\text{SIGaAs}}]$ layer lattice constant perpendicular to the surface as a function of layer thickness, a) 295 K, b) 77 K after cooling in dark, c) 77 K after cooling in dark and 5 min. illumination, d) 77 K after cooling in dark and 15 min. illumination. Thickness $d = 2 \mu\text{m}$ at the interface and $d = 0 \mu\text{m}$ at the free surface.

from high values at the interface to low values at free surface of the layer (fig.3a). Rocking curves taken after cooling in darkness show only slight change of the lattice parameter (fig.3b). There is lowering of the values at free surface in fig.3b which overlaps with fig.3a close to the interface. Illumination at 77 K resulted in radical change of the profile with pronounced changes of the lattice parameter close to the interface and free surface (fig.3c). In this case lattice parameter at free surface continue to drop to smaller values but there is an increase of the lattice parameter at the interface. This type of profile we predict for curves as in fig.1c and fig.2c. If the illumination is prolonged as for fig.2d we predict from our calculation the profile to be more steep and with smaller values at the free surface combined with further increase of lattice mismatch at the interface (e.g. fig.3d). All in all it shows that for LT GaAs layers EL2-like defects when transferred to the metastable state induce considerable strain near interface increasing with the number of defects transferred. Another interesting result seen clearly at fig.3 is that mean value of the lattice mismatch in the layer tends to be stable all the time (cross point of the profiles).

Conclusions

Main results of our experiments can be summarized as follows: 1) X-ray experiment can be successfully employed as a tool for metastable behavior studies of EL2-like defects in LT GaAs (already established for EL2 in SI GaAs and D^0 centers in GaAlAs), 2) gradient of the lattice parameter perpendicular to the layer is present for as grown LT GaAs, 3) there is a considerable build up of the strain especially near the interface of the layer when EL2 type defects (arsenic antisite) are transferred to the metastable state. Strain which is present in as grown LT GaAs layers seem to play dominant role

in the results reported so far for those materials. Differences between behavior of the EL2 defects in SI GaAs substrates and in LT GaAs in various experiments could be ascribed to the strain presence as well. Bragg peaks broadening for LT GaAs and narrowing for the substrate one is clearly connected with highly strained layer in first case and possibility of lattice relaxation in bulk material. Difference in wavelength causing quenching of the absorption spectrum for LT GaAs and SI GaAs points to the more energetic photons needed for metastable transfer in LT GaAs which are essential for overcoming present strain. The fact that LT GaAs absorption spectrum is not fully quenchable indicates that available photon energy can not overcome strain barrier and defect can not be moved to the metastable position in the lattice. Possibility of the recovery from the metastable state by illumination with 1350 nm wavelength for LT GaAs (not observed in SI GaAs) is probably also caused by the highly strained layer, while in SI GaAs metastable lattice position of the defect requires considerably more energy to do so and in such a way this position seem to be different than in LT GaAs. Last but not least EPR signal not optically quenchable for LT GaAs might be also connected with the strain barrier which was already suggested in [2].

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SURFACE ACOUSTIC WAVE DETECTION OF LARGE LATTICE RELAXATION OF METASTABLE EL2 IN LT-GaAs

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ABSTRACT

For the first time, surface acoustic waves (SAWs) were used to study the lattice relaxation of metastable defects. A persistent increase of as much as 0.4% of the SAW velocity at low temperatures was observed after illumination of LT-GaAs; this increase could be quenched by annealing at 120-1300K. This behaviour is caused by the metastable transition of EL2-like As_{Ga} defects and constitutes the direct experimental proof of the illumination induced large lattice relaxation of this defect.

INTRODUCTION

GaAs, grown by molecular beam epitaxy (MBE) at very low temperatures (LT-GaAs) between 200° and 300°C has a number of unusual properties, which make it a technologically important material, particularly when used to eliminate sidgating and backgating in GaAs integrated circuits [1]. Its most important property is the presence of as much as 1% superstoichiometric As [2,3], which in as-grown layers is incorporated as As_{Ga} antisite defects. As_{Ga} in LT GaAs has properties very similar to those of EL2 in bulk GaAs [4,5] giving rise to the similar spectral shape of the optical absorption band, which is quenchable by illumination at low temperatures [6].

For the first time, the metastability of EL2 in LT-GaAs is studied with the surface acoustic waves. SAWs, similar to ocean waves, propagate parallel to the surface, but decay with depth so that all displacements are essentially zero at a depth of about one wavelength [7,8]. The displacements in the SAW are both longitudinal and transverse, each with its own variation of magnitude vs. depth. The SAW can be of particular importance as a tool to study illumination induced persistent lattice rearrangement of metastable defects. The lattice rearrangement causes a change in elastic constants, which can be directly measured by the SAW techniques. The SAW measurements can therefore provide unique information on the mechanism of defect metastability, an issue of great current interest.

A surface acoustic wave delay line [9] was used to measure the SAW velocity and propagation loss. It consists of two periodic gratings of electrodes of alternating polarity (called interdigital transducers, IDTs) as source and as detector of the SAW (Fig.1). Excitation and detection of the SAW is due to the piezoelectric character of GaAs. From the condition of constructive interference of the SAWs launched from the individual fingers of the IDT, it follows that the excitation of the SAW is the most efficient if

$$f_0 = v/\lambda \quad (1)$$

where f_0 is the SAW frequency, v is the SAW velocity and λ is the IDT period. The frequency dependence of transmission s_{21} of the delay line of Fig. 1 can be measured with a network analyser and is ideally [10,11]

$$|s_{21}(f)| \sim (\sin x/x)^2 \quad (2)$$

where $x = N\pi(f - f_0)/f_0$, N being the number of finger pairs in the IDT. The SAW velocity can be obtained from eq. (1) as a product of the IDT period and the frequency corresponding to the maximum transmission $s_{21}(f)$ of the delay line.

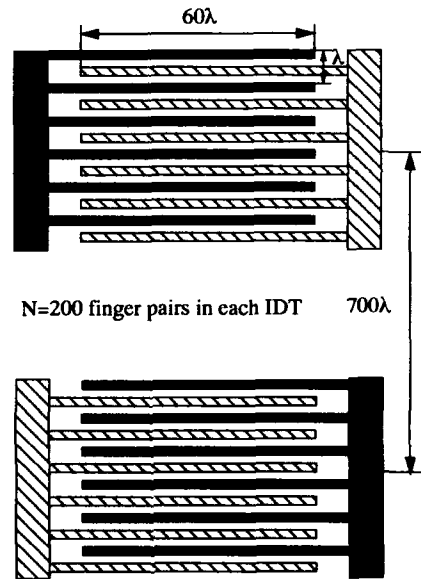


Fig. 1 Surface acoustic wave bandpass filter/delay line design used in this work.

While the absolute value of the SAW velocity can be determined from the network analyser measurements using eq. (1) with a precision of the order of 10^{-4} , a minute change of 10^{-7} in SAW velocity with temperature or illumination can be detected. For that purpose, the SAW delay line is converted into a SAW oscillator by introducing positive feedback [10]. The high sensitivity to minute changes in SAW velocity is a result of the oscillation frequency stability of $\delta f/f = 10^{-7}$. The frequency of the oscillation satisfies the resonance condition that the phase shift around the loop is a multiple of 2π radians

$$2\pi fL/v + \phi_E = 2\pi n \quad (3)$$

where n is an integer and ϕ_E is the electrical phase shift associated with electrical components. A change in SAW velocity v causes the same relative change in oscillation frequency f , so that the phase shift (3) remains unchanged. From the combination of frequencies satisfying eq. (3) with different integer values of n , the operating frequency of the oscillator would be the one corresponding to the maximum transmittance s_{21} .

EXPERIMENTAL

A $6\mu\text{m}$ GaAs epilayer (0.3λ thick), grown by MBE on semiinsulating (001) cut GaAs substrate was used in this work for SAW delay line fabrication. The delay lines were fabricated by standard chlorobenzene lift-off photolithography, with 16 devices on each 2" wafer. The SAW delay lines were oriented along $\langle 110 \rangle$ direction, the direction of maximum electromechanical coupling coefficient and zero beam steering angle in the (001) plane of GaAs. Since approximately 3/4 of the elastic energy of the surface acoustic wave on GaAs is localized within the top 0.3λ thick layer (as one can estimate from the published depth profiles of particle displacements [12]) the SAW velocity on a 0.3λ epilayer of LT GaAs on GaAs substrate is quite close to the SAW velocity in the theoretical limit of an infinitely thick epilayer. The parameters of the SAW delay line used are indicated on Fig. 1. The frequency responses of the SAW delay lines were measured on an HP4195A network analyser and stored on a floppy disk. The positive feedback loop needed to operate the device as an oscillator consisted of an amplifier cascade, a variable attenuator and a power splitter, which branched off half of the power to an HP5343A microwave frequency counter.

The epilayer contained 0.8% superstoichiometric As, as established by particle induced X-ray emission spectroscopy. The optical absorption spectrum was characteristic for EL2 [5] with a room temperature absorption coefficient of $2.8 \times 10^3 \text{ cm}^{-1}$ at $1 \mu\text{m}$.

RESULTS

Arsenic superstoichiometry related SAW velocity decrease

The SAW velocity (for $\lambda=20\mu\text{m}$) on a $6\mu\text{m}$ LT MBE epilayer grown on SI GaAs was 2832.9 m/s at the room temperature of 291°K . This velocity is 1.2% smaller than the SAW velocity of the substrate alone. The measured value of the SAW velocity on the substrate, 2868.4 m/s , is in an excellent agreement with the reported value of 2868 [12]. After the SAW device is annealed in a nitrogen atmosphere, reducing the superstoichiometric arsenic concentration [2,3], the SAW velocity becomes closer to that of the substrate alone. The SAW velocity was 2841.5 , 2849.2 and 2854.8 m/s for the samples annealed at 350°C for 20min, at 400°C for 20min and at 435°C for 10min, respectively. Loss of As after anneals could be directly observed from pitting of the Al metallization of the SAW devices and appearance of a greyish colour in the vicinity of the pits.

The SAW velocity increase upon the metastable transition of EL2

The SAW velocity of as-grown LT GaAs at helium temperatures persistently increases by up to 0.42% after illumination for 1 hour with the white light from a halogen 250W lamp (Figs.2,3). The absence of the persistent change in photoconductivity proves that the observed persistent increase in the insertion loss of the SAW device is entirely due to elastic effects. At the same time, the insertion loss of the SAW delay line increases after illumination (Fig. 3).

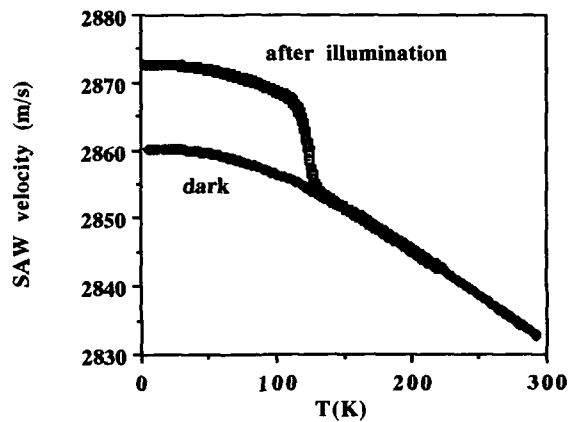


Fig. 2. Temperature dependence of the SAW velocity ($\lambda=20\mu\text{m}$) on the $6\mu\text{m}$ thick as-grown LT GaAs cooled in the dark (lower curve) and illuminated by white light from the halogen lamp (upper curve). The SAW oscillator was used for the measurement.

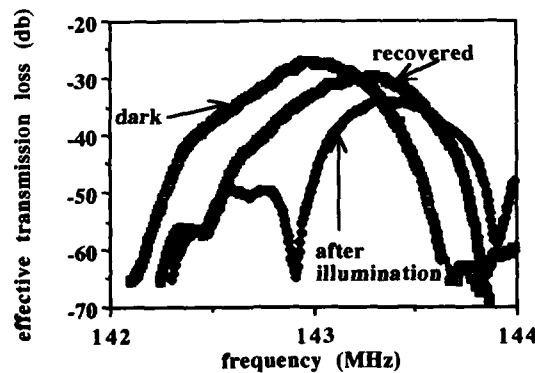


Fig. 3. Frequency response of effective transmission loss of the SAW filter on Fig.1 implemented on as-grown epilayer at 11K. The responses after cooling in the dark (step 1), after photoquenching with 1.38eV light (step 2) and after optical recovery with 0.95eV light (step 3) following step 2 are shown.

The dark values of the SAW velocity and delay line insertion loss can be recovered only by annealing the sample at 120-130K (Fig. 2), which coincides with the temperature range of EL2 recovery from the metastable state [5]. The return of EL2 from the metastable to the ground state for the case of LT GaAs can be induced not only thermally but also optically for illumination with low energy light (for example, 1.3 eV). This optical recovery of EL2 was observed in this work after EL2 had been photoquenched as an illumination induced decrease of the SAW velocity (Fig.3). To explain the decrease in transmission upon EL2 photo-quenching, one should consider the masking action of the IDT metallization. Indeed, only the area in the spacings between IDT fingers was exposed to illumination as the result of which the SAW velocity there increases. At the same time the area underneath the fingers is not exposed to illumination and the SAW velocity there remains unchanged. In this way, an "elastic grating" is created. The elastic grating causes increased reflection of the SAW from the IDT fingers and consequent decrease in transmittance. In agreement with this model, no decrease in transmittance was observed when the sample was illuminated from the back.

DISCUSSION

First, the observed slower SAW velocity on LT GaAs compared to bulk GaAs can be read explained if most of the superstoichiometric As incorporates as As_{Ga} antisites. Indeed, due to two excess electrons of As compared to Ga, which occupy the antibonding orbitals, the As_{Ga} -As bonds are softer compared to the Ga-As bonds. The softer bonds result in smaller elastic constants and consequently smaller SAW velocity. One can roughly estimate that presence of two antibonding electrons in addition to two bonding electrons would decrease the spring constant of the bonds by approximately 1/4.

The persistent increase in the SAW velocity of LT-GaAs at low temperatures constitutes a clear proof of the large lattice relaxation of EL2 and can serve as the experimental test of the latest model of EL2 metastability [13]. According to this model, the metastable transition of EL2 is accompanied by breaking one of the four bonds of As_{Ga} antisite defect while reinforcing the remaining three bonds. The direction of the SAW velocity change can be predicted theoretically by the model [13] and should be compared with the result in this work.

Finally, it is worth pointing out that the surface acoustic wave technique opens the door to further highly precise measurements of the influence of external perturbations, such as illumination, temperature changes, high temperature anneals and magnetic and electric fields on elastic properties of thin films. It can be expected that the surface acoustic wave technique will find its place as a tool for materials research of thin film structures.

ACKNOWLEDGMENT

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DEFECT MODEL AND GROWTH CHARACTERISTICS OF LOW TEMPERATURE GaAs

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ABSTRACT

Low-temperature GaAs layers (LTGaAs) grown by molecular beam epitaxy on GaAs substrates have been characterized by x-ray diffraction techniques. X-ray rocking curve measurements on more than 200 anneal conditions show that through appropriate choice of growth condition, layers with different states of strain are obtained. Three distinct ranges of low temperature growth are defined, labelled as "low-range," "mid-range," and "high-range," corresponding to growth temperatures less than 260 °C, between 260 and 450 °C, and more than 450 °C, respectively. 0.5 μm thick films grown in the low-range are amorphous, whereas those in the mid-range are fully strained and lattice-matched to the substrate, and those grown above 450 °C are indistinguishable from ordinary GaAs. Notable properties of mid-range layers are the random behavior of the as-grown strain, and the expansion and contraction of the lattice parameter with thermal anneals up to 900 °C. A growth model for LTTGaAs based on arsenic antisite defects is proposed.

INTRODUCTION

The molecular beam epitaxy (MBE) growth of As rich GaAs layers at low temperatures on GaAs (LTGaAs) was reported recently¹⁻³. The interesting physical and electronic properties of these and similar low-temperature III-V compounds make the materials potentially useful for a wide range of device applications. Among these properties are reduced recombination times of about 400 fs, suitable for integrated sub-picosecond optoelectronic switches, and their high breakdown voltage, useful for power field effect transistors (FET's).^{4,5} It was shown by transmission electron microscopy in Ref 1 that the layers are highly perfect and contain only a few dislocations. In addition, x-ray rocking curves from a sample grown at 200 °C showed a second diffraction peak at an angle slightly lower than that of the substrate. This peak was interpreted as that of a relaxed cubic lattice with a lattice parameter slightly larger than, and supported by the GaAs substrate which is also cubic. However, an interface dislocation network which is nearly always present in mismatched systems was not reported. The concept of a relaxed cubic lattice appeared to be in conflict with the absence of misfit and threading

dislocations, as seen from transmission electron microscopy (TEM). A study of the behavior of the lattice parameter and electrical properties was also reported recently.⁶ In our study, these findings were examined in greater detail. In particular, we wished to ascertain the possibility of a wider range of growth temperatures about 200 °C for this material. It was also desirable to calibrate the growth temperatures more exactly, so that wafers obtained from different sources could be compared in a meaningful way. Although our findings in general agreed with earlier work regarding the perfection of the layers and the double peaking in x-ray rocking curves, they differed in other respects, including the observation of tetragonal distortion, which accounts for the high perfection of the layers in the absence of extended defects, and the interpretation of the expansion and contraction of the buffer layer lattice with thermal anneal, consistent with a model involving As_{Ga} defects. These observations are briefly reported here.

EXPERIMENT

Epitaxial layers of low-temperature GaAs, 0.5 μm thick, were grown on semi-insulating GaAs substrates in a VG V80H MBE system. All layers were grown according to customary, well known procedures in cleaning, preheating, post-growth cooling, and overall handling of the substrates. Substrate temperatures ranging from 150 to 500 °C were investigated. Growth temperatures were measured through a thermocouple which in this instrument was located as close to the sample holder as possible without actual contact. The temperatures reported here are somewhat different from other published data, probably because of calibration differences among various instruments. Although the accuracy of thermocouple data may be uncertain, relative changes in temperature in one instrument are considered to be reliable.

To better understand the defect structure and growth mechanism in LTGaAs, annealing effects were included in this study. Rapid thermal annealing (RTA) and furnace annealing (FA) were performed at temperatures ranging from 300 to 900 °C in steps of 50 °C in a forming gas atmosphere (90% N_2 , 10% H_2). The anneal time at temperature was 10 minutes for both RTA and furnace annealing. The samples were sandwiched between two GaAs wafers to prevent the escape of As during the anneal. The crucible containing the samples to be furnace annealed was inserted into a quartz tube which was initially raised to the desired temperature. However, the furnace temperature dropped by several tens of degrees Celsius after the samples were inserted. Hence, these samples were subjected to additional heating at lower temperatures for periods of up to 15-20 minutes, before the furnace returned to equilibrium temperature. X-ray measurements were performed on a Blake double crystal diffractometer, equipped with a Si(100) beam conditioner as the first crystal which was adjusted for the (004) reflection of $CuK\alpha_1$ radiation. The incident beam size was 0.4 mm wide x 0.5mm high which, depending on the angle of

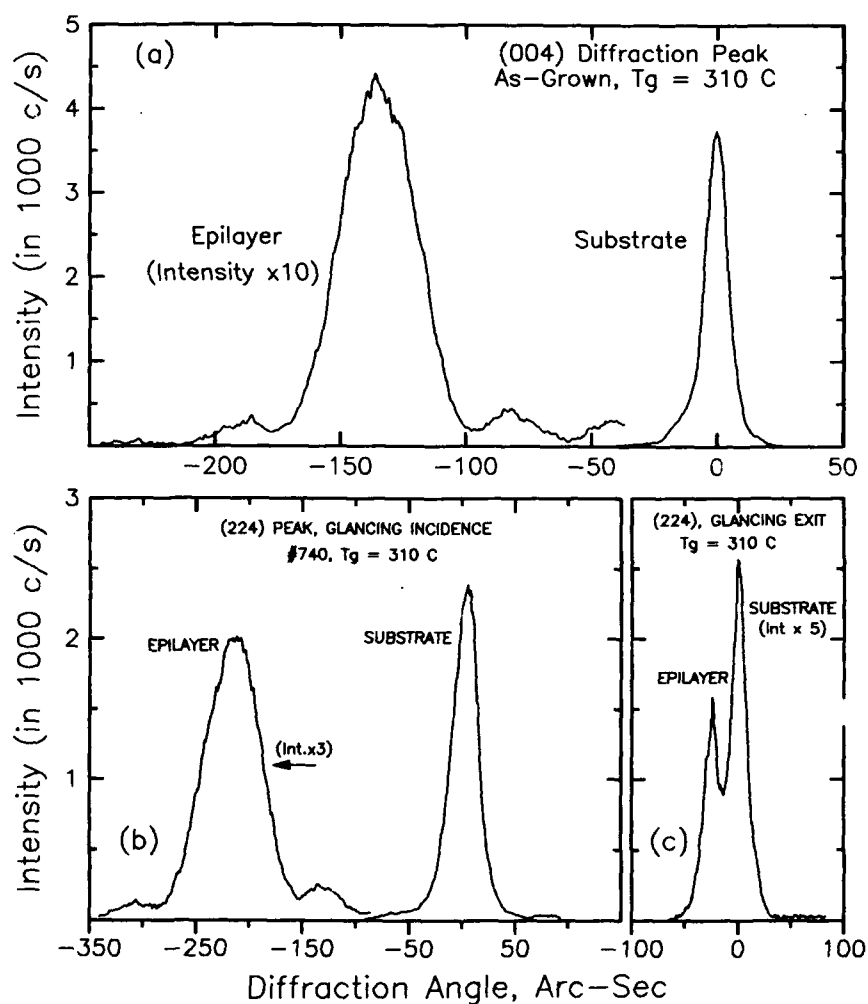


Fig. 1- X-ray rocking curves of LTGaAs on GaAs. a- symmetric (004) reflection, b- asymmetric, glancing incidence (224) reflection, and c- asymmetric, glancing exit (224) reflection.

incidence, covered a sample area approximately 0.4 to 3 mm wide.

RESULTS AND DISCUSSION

On the basis of x-ray measurements on samples grown at temperatures between 100 and 500 $^\circ\text{C}$, three ranges of low-temperature growth were established, labelled for convenience as the "low-range," $T_g < 260^\circ\text{C}$, the "mid-range," $260^\circ\text{C} < T_g < 450^\circ\text{C}$, and the "high-range."

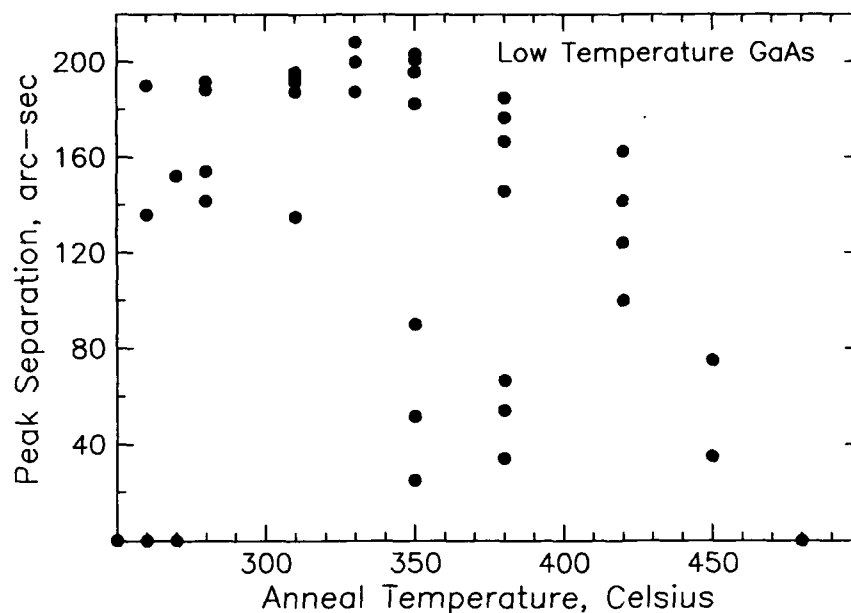


Fig. 2- Variation of the rocking curve peak separation for different growth temperatures in as-grown LTGaAs.

with $T_g > 450^\circ\text{C}$. Samples in both the low- and the high-range showed only one diffraction peak from the substrate lattice parameter alone, while those in the mid-range gave two peaks corresponding to both the substrate and the epilayer. Because of the complexity of the data, only the mid-range samples are analyzed in the present paper. A more detailed discussion and analysis including the remaining groups will be presented elsewhere.⁷ X-ray analysis was based on measuring one (004) and two (224) rocking curves, the latter in both "glancing incidence" and "glancing exit" geometries (Fig. 1). Since it was determined that the layers were not tilted with respect to the substrate, only one (004) rocking curve was used to measure the perpendicular lattice parameter.⁸ Varying and unpredictable rocking curve peak separations were often observed for the same growth temperature T_g . Repeated tests were made to determine the range of the strains. Fig. 2 shows the measured separations observed so far, as a function of T_g using the (004) data. A full discussion of this phenomenon is also outside the scope of the present paper. It is possible that the clustering of the data in two relatively broad bands may be due to a metastable process which produces different levels of strain with small perturbations in growth conditions.

For annealing studies, samples were chosen from those shown in Fig. 2 to cover a broad range of initial strains. Rocking curve measurements on these samples showed a complex pattern

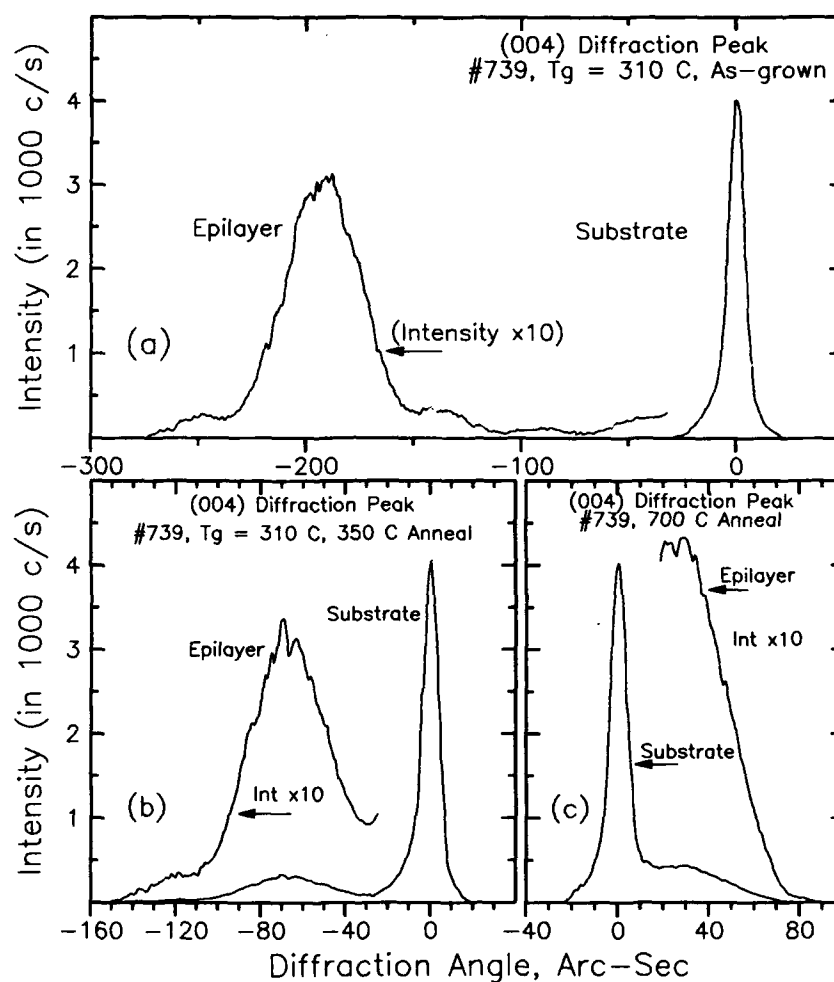


Fig. 3- Shift of the epilayer diffraction peak with anneal in LTGaAs; (004) rocking curves. a- As grown material; b- Furnace-annealed at 350 °C for 10 minutes; c- Furnace annealed at 700 °C.

of expansion and contraction of the vertical lattice parameter. Figs. 3 a-c show x-ray rocking curves obtained from a sample grown at 310 °C in the as-grown condition and after furnace anneal at 350 and 700 °C, respectively. Typical strain plots obtained from similar rocking curves are shown in Fig. 4. The initial values of vertical strain ϵ_{\perp} were positive for all samples, denoting an expansion of the epilayer relative to the substrate. Thermal annealing at temperatures less than 700 °C gradually reduced the mismatch. Aside from random experimental variations, most samples annealed at temperatures between 400 and 600 °C were lattice-matched to the substrate.

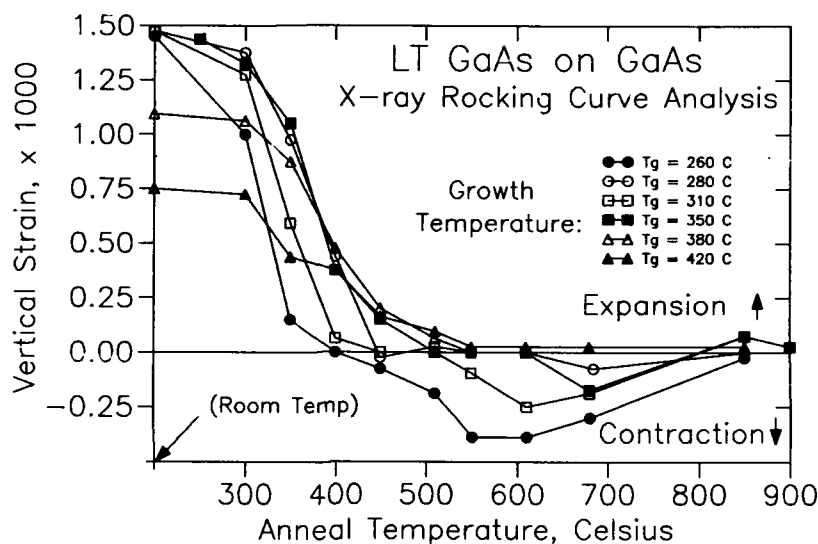


Fig. 4- Strain plots as a function of anneal temperature for several samples grown between 260 and 420 °C.

For some layers, annealing at higher temperatures such as 700 °C caused a contraction of the lattice, while for other layers no further change in the lattice parameter was detected. The latter group consisted mainly of samples whose initial, pre-anneal vertical strain was significantly lower than the observed maximum (0.15%). This, however, is not the general rule: some of the samples with initially large strains showed only a gradual relaxation without further contraction. Continued annealing at higher temperatures resulted in contraction not exceeding 0.04%. A second lattice matching was then observed near 850 °C (Fig 4). Some of the samples exhibiting this initial contraction were further annealed at temperatures of up to 900 °C, upon which they showed a slight expansion. Changes in the in-plane lattice parameter and the equivalent bulk (relaxed) lattice parameter were also evaluated assuming that the elastic constants for these layers are nearly the same as for pure GaAs.⁷ While in most cases the epilayer was found to be fully strained, a small mismatch was occasionally observed.

Electron diffraction x-ray analysis (EDXA) was used to compare the level of arsenic before and after anneal in several samples. Although the technique has limitations in giving absolute values of elemental composition, it can be used in a comparative sense with reasonable accuracy. Thus, the atomic fractions of Ga and As in reference GaAs wafers computed by the instrument were typically about 60% and 40%, respectively. The difference between the calculated ratio

and the expected "50-50" composition was consistent for all standard samples. When wafers bearing LTGaAs epilayers were measured, the As content was found to be higher than the standard by about 3% on the epilayer side (facing the source), and 2% on the substrate side (away from the source). Both annealed and unannealed samples gave similar results. The similarity of the As level on both sides of the wafers suggests that the excess arsenic, although an indicator of overpressure, cannot entirely represent a structural defect responsible for changes in the lattice parameter and strain in LTGaAs layers. This finding may explain the presence of large As aggregates which are sometimes observed in these materials.¹

THE GROWTH MODEL

The proposed growth model for LTGaAs is based on a consideration of annealing phenomena from the standpoint of two As-type defects, i.e., As_{Ga} antisites and interstitials. A rough estimate suggests that the antisite defects alone can account for most of the observed variations in the strain. According to this estimate, the internal pressure in the GaAs lattice, comparable to its bulk modulus of approximately 7.5×10^{11} dynes/cm², is balanced by the repulsive force of the five-atom cluster of As atoms at each defect site. Assuming that the cluster is contained within a spherical volume with its center at the As_{Ga} , a defect volume of approximately 185 \AA^3 is calculated, compared to 60 \AA^3 in the absence of the defect. The resulting total volume of 305 \AA^3 corresponds to a lattice parameter of 6.73 \AA or an effective lattice parameter expansion of 19%. Although this calculation is highly approximate, it reflects the magnitude of the expansion which would have to be accommodated by the LTGaAs lattice as a whole. In a crystalline layer constrained to be lattice-matched to the substrate, the expansion follows tetragonal distortion, and is controlled by the elastic constants of the epilayer-substrate system. The maximum bulk lattice expansion in the "free standing" LTGaAs lattice is thus 0.08%, using our largest rocking curve peak separation of nearly 200 arc-sec.¹ Hence, the average fraction of unit cells containing As_{Ga} defects is about 0.004, obtained from the ratio of the bulk strain to the unit cell expansion, or about $2 \times 10^{19} \text{ cm}^{-3}$. We note that this is an estimate of the density of the unit cells containing defects per unit volume, and is consistent with earlier estimates based on EPR data.¹

The following model is therefore proposed for the growth process and the defect structure in LTGaAs. During the arsenic-rich, low-temperature deposition, antisite As_{Ga} defects are formed which expand the lattice. The epilayer is tetragonally distorted, with a vertical lattice parameter larger than the substrate. Following anneal at temperatures approximately 200 °C higher than T_p , antisite As_{Ga} defects are partially removed, thus reducing the vertical strain. Ga vacancies generated in this process are not immediately filled, but remain in the lattice at somewhat higher anneal temperatures. A combination of Ga vacancies and residual antisite defects is formed, yielding

a lattice which is nearly fully matched to the substrate in both in-plane and vertical directions. Additional anneal at higher temperatures removes nearly all the antisite defects. The epilayer lattice contracts, reaches a minimum, and exhibits a negative strain. Upon annealing at temperatures near 900 °C, Ga vacancies are removed through localized, short range dislocation loops. This coalescence gives rise to interstitial As atoms which may then increase the average lattice parameter, as demonstrated by x-ray data.

CONCLUSIONS

In this paper, several aspects of low temperature growth of GaAs layers on GaAs substrates were investigated. A growth model for LTGaAs was proposed, consistent with the picture of the modulation in the LTGaAs lattice parameter with thermal anneal. It was found that the layers grown at temperatures between 260 and 450 °C have a bulk lattice parameter larger than the substrate, but are lattice-matched to it in the in-plane direction. The increase in the lattice parameter was seen to be consistent with the effect of As_{Ga} antisite defects, at a level nearly equal to that estimated by other techniques. Comparable levels of excess arsenic were measured on both sides of the grown wafers, independent of the anneal conditions. Hence, the major structural defect in LTGaAs is formed only by a small fraction of the environmental As in the form of arsenic antisites.

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AN INVESTIGATION ON THE LATTICE SITE LOCATION OF THE EXCESS ARSENIC ATOMS IN GaAs LAYERS GROWN BY LOW TEMPERATURE MOLECULAR BEAM EPITAXY.

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ABSTRACT

We have measured the excess As atoms present in GaAs layers grown by molecular beam epitaxy at low substrate temperatures using particle induced x-ray emission technique. The amount of excess As atoms in layers grown by MBE at 200°C were found to be $\sim 4 \times 10^{20} \text{ cm}^{-2}$. Subsequent annealing of the layers under As overpressure at 600°C did not result in any substantial As loss. However, transmission electron microscopy revealed that As precipitates (2-5 nm in diameter) were present in the annealed layers. The lattice location of the excess As atoms in the as grown layers was investigated by ion channeling methods. Angular scans were performed in the $\langle 110 \rangle$ axis of the crystal. Our results strongly suggest that a large fraction of these excess As atoms are located in an interstitial position close to an As row. These As "interstitials" are located at a site slightly displaced from the tetrahedral site in a diamond cubic lattice. No interstitial As signal is observed in the annealed layers.

INTRODUCTION

GaAs thin films grown by Molecular Beam Epitaxy (MBE) at low growth temperature, T_g ($< 400^\circ\text{C}$) have been subject to many investigations recently [1-10]. Murotani *et al.* [11] first reported the development of this material in 1978 and predicted it to be a useful buffer materials for GaAs field effect transistors (FET). Smith *et al.* [1] have successfully used the low temperature MBE (LTMBE) GaAs as buffer layers for the fabrication of GaAs FET's and showed that the LTMBE-GaAs layer eliminates backgating between the devices. In addition to its great technological potential, the LTMBE-GaAs layers also have many interesting material properties such as high defect concentration, high electrical resistivity and are therefore of scientific interest as well. Previous reports revealed that LTMBE-GaAs layers grown at substrate temperatures in the range of 200-250°C are high quality single crystals with > 1 atomic % excess As [1-3]. These layers have lattice parameters larger than that of a normal GaAs crystal by $\sim 0.1\%$ as measured by x-ray rocking curve experiments. The breakdown of the crystallinity in these layers occurs at growth temperature below 200°C [6]. At $T_g < 200^\circ\text{C}$, only a thin layer ($< 2 \mu\text{m}$) of good quality GaAs can be grown before a high density of "pyramidal" defects nucleates and columnar polycrystalline growth starts.

Electron paramagnetic resonance measurements on LTMBE-GaAs layers showed that these layers have $\sim 5 \times 10^{18} \text{ cm}^{-3}$ As antisite defects [2]. In addition, they are also found to be highly resistive and possess no measurable photoluminescence signal [1]. Subsequent annealing of these layers above 400°C in As overpressure results in a uniform semi-insulating property and the lowering of their lattice parameter to the value of stoichiometric GaAs grown at normal temperatures ($\sim 600^\circ\text{C}$). Transmission electron microscopy (TEM) investigation revealed that As precipitates with diameter ranging from 2 to 5 nm are formed in the layers after annealing [2-5]. The As precipitates formation in the LTMBE layers has been studied in detail by many investigators [4,5,8]. Recently, it has also been speculated that the semi-insulating nature of the annealed LTMBE-GaAs layers is the result these As precipitates [5].

In this paper we report on an investigation of the LTMBE-GaAs layers grown at $T_g = 200^\circ\text{C}$ using ion beam techniques, namely, particle induced x-ray emission (PIXE), Rutherford backscattering spectrometry (RBS), and the combination of these techniques with ion channeling. Our study addresses on the issues of stoichiometry, defects arising from the off-stoichiometry, and the lattice location of excess As in the layers.

EXPERIMENTAL PROCEDURES

The LTMBE-GaAs layers were grown on semi-insulating liquid-encapsulated Czochralski (100) GaAs substrates. The samples were grown using a Varian GEN II MBE system at $T_g \approx 200^\circ\text{C}$ with a growth rate $\sim 1\mu\text{m/hr}$. The thickness of the layers grown is $\sim 2\text{--}3\mu\text{m}$. Some of the layers were annealed at 600°C in the MBE chamber with an As overpressure. The stoichiometry of LTMBE-GaAs layers was measured by PIXE using a 1.2 MeV H^+ beam with samples tilted at $60\text{--}70^\circ$ with respect to the ion beam. The beam energy and the tilt angle were chosen so that the x-ray emitted by the substrate GaAs is $< 10\%$ of the total collected x-ray signals. The x-rays emitted were detected by a Si(Li) detector located at 30° with respect to the ion beam.

The crystallinity and the depth profile of crystalline defects in the LTMBE-GaAs layers were characterized by RBS in the channeling orientation using a $1.95\text{ MeV }^4\text{He}^+$ beam. Back-scattered particles were analyzed by a Si surface barrier detector located at 165° with respect to the ion beam. The samples were mounted on a two-axis goniometer for alignment. The lattice location of the excess As atoms in the LTMBE-GaAs layers grown at 200°C was studied by PIXE/channeling using a 0.5 MeV H^+ beam. The ion beam was aligned along the $\langle 110 \rangle$ axis of the layer. Angular scans were obtained by tilting the sample parallel to a $\{110\}$ plane across the $\langle 110 \rangle$ axis and measuring the $\text{GaK}\alpha$ and $\text{AsK}\beta$ x-rays. The x-ray yields at each tilt angle were normalized by the values obtained when the ion beam was not aligned with any axis of the sample, i. e., in a random direction.

RESULTS AND DISCUSSION

Figure 1 shows the $\text{GaK}\beta$ and $\text{AsK}\alpha$ x-rays obtained by PIXE for a LTMBE GaAs layer ($T_g=200^\circ\text{C}$) and the bulk GaAs standard normalized by the $\text{GaK}\alpha$ x-ray (not shown in the figure). The higher $\text{AsK}\alpha$ x-ray yield from the LTMBE layer indicates the presence of excess As in the layer. Over 10^6 counts of $\text{GaK}\alpha$ and $\text{AsK}\alpha$ x-rays were accumulated. The relative composition of the layer $[\text{As}]/[\text{Ga}]$ is calculated by taking the ratio of the total measured $\text{AsK}\alpha$ and the $\text{GaK}\alpha$ x-rays and comparing this ratio to that obtained for a bulk GaAs standard. Since the $\text{GaK}\beta$ and the $\text{AsK}\alpha$ x-rays are not resolved, it is necessary to subtract the $\text{GaK}\beta$ x-ray from the total yield in order to obtain a more accurate $[\text{As}]/[\text{Ga}]$ ratio. This is carried out by assuming a fixed $\text{GaK}\beta/\text{GaK}\alpha$ yield ratio. The overall statistical error associated with this measurement is estimated to be $\sim 0.2\%$. The amount of excess As, $\Delta[\text{As}] = ([\text{As}] - [\text{Ga}])/([\text{As}] + [\text{Ga}])$, in this case is ≈ 0.01 ($\approx 4 \times 10^{20}$ atoms/ cm^3). The effect of annealing on the stoichiometry of the LTMBE layers is also studied. PIXE results show that when the layers were annealed under an As overpressure, there is no significant change in $\Delta[\text{As}]$ up to an annealing temperature of 600°C .

X-ray rocking curve measurements on the unannealed LTMBE layers show that the lattice parameter, a of the layers is considerably larger than that of a normal GaAs crystal, a_b [2,6,7]. The deviation in the lattice parameter, $\Delta a = (a - a_b)/a$, is found to be $\sim 0.2\%$. Therefore, the PIXE and x-ray results show that more excess As is incorporated into the layer at $T_g = 200^\circ\text{C}$ and that the dilation of the lattice parameter in the layers can be attributed to the presence of excess As atoms in the layer.

Rocking curve measurements [7] on samples annealed in As overpressure show that the lattice parameter of the layers gradually decreases as the layers are annealed at temperatures higher than 300°C and finally resume the bulk value when the annealing temperature reaches 450°C . Since no As loss can be detected by PIXE, the excess As atoms are believed to coalesce forming As precipitates in the layer and thus returning the lattice parameter to a_b . This is

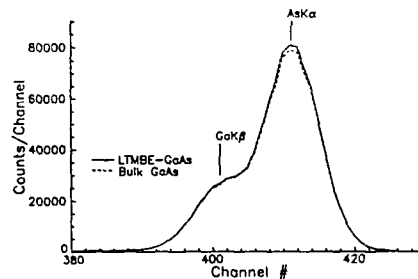


Fig.1 1.2 MeV H^+ PIXE spectra from the bulk GaAs standard and a LTMBE GaAs layer grown at $T_g=200^\circ\text{C}$. Only the $\text{GaK}\beta$ and $\text{AsK}\alpha$ peaks are shown in the figure.

confirmed by TEM experiments which observed small As precipitates (2-3 nm in diameter) in a LTMBE layer ($T_g=200^\circ\text{C}$) annealed at 450°C under As overpressure [8].

For LTMBE layers grown at $T_g \geq 200^\circ\text{C}$, the RBS/channeling spectra are very similar to that of the bulk GaAs sample with slightly higher dechanneling in the spectra from the layer as the ions penetrate deeper into the layer. Fig. 2 shows the $\langle 110 \rangle$ aligned RBS spectra from a bulk GaAs and a LTMBE layer grown at $T_g=200^\circ\text{C}$ as grown and annealed at 600°C under As overpressure. Note that except for the higher dechanneling rate in the spectra from the layers, all the spectra are very similar to the bulk one indicating that the layers have good crystalline quality. Since TEM experiments did not reveal any extended defects in these layers, we can assume that the higher dechanneling rates in the layers are due to point defects. The concentration of point defects can be calculated from the RBS/channeling spectra as outlined in Feldman *et al.* [12]. The point defect concentrations in the as-grown and annealed layers calculated from the data in Fig. 2 are shown in Fig. 3. A uniform distribution with $n_D \sim 1.7 \times 10^{20} \text{cm}^{-3}$ is observed in the as-grown layer. This value of n_D is lower than the total excess As concentration measured by PIXE in this layer ($\sim 4.0 \times 10^{20} \text{cm}^{-3}$). The n_D for the annealed sample increases from $\sim 1 \times 10^{20}$ at the surface to a constant value of $\sim 4.6 \times 10^{20} \text{cm}^{-3}$ at $0.4 \mu\text{m}$ depth. This saturated value of point defect density agrees very well with the excess As concentration in the layer, indicating that most of the excess As in the annealed layer exist in the form of random point defects contributing to the dechanneling of the ion beam. TEM on this layer revealed that small As precipitates (2-3 nm in diameter) are present in this layer. These precipitates are either amorphous or "pseudocubic" constrained by the GaAs host crystal [8]. These observations are in good agreement with the RBS/channeling results. The fact that the n_D in the as-grown layer is much lower than the excess As concentration suggests that the excess As in the as-grown layer may be in the Ga sites or sitting in specific sites close to the normal host sites and therefore with a dechanneling factor, σ_D smaller than that of a random point defect. To investigate the lattice location of the excess As atoms in the layer, PIXE/channeling experiments were also carried out.

Figure 4 shows the angular scans of the $\text{GaK}\alpha$ and $\text{AsK}\beta$ x-rays across the $\langle 110 \rangle$ axis along a $\{110\}$ plane from (a) the bulk GaAs standard and (b) the as-grown LTMBE layer. The $\langle 110 \rangle$ axis is chosen since the Ga and As atoms form separate rows in this direction [12,13] defining two separate channels, one bound by three Ga rows and the other by three As rows. Since the critical angle for channeling ψ is proportional to the square root of the atomic number Z_2 of the target atoms forming the channel, i.e. $\psi \propto Z_2^{1/2}$ [12] the values of the ψ for the scans arising from the $\langle 110 \rangle$ channel as defined by the Ga and As strings should be different. In this case, $\psi(\text{Ga})/\psi(\text{As}) \propto \sqrt{(31/33)} = 0.97$. The critical half angle $\psi_{1/2}$ of the scans is defined as the angular deviation between the channeled direction and the angle at which the x-ray yield is equal to half of the value when the alignment of the beam is far from the axial channel. Since $\psi_{1/2} \propto \psi$, the measured $\psi_{1/2}$ values are also $\propto Z_2^{1/2}$. Table I summarizes the average $\psi_{1/2}$'s of the $\text{GaK}\alpha$

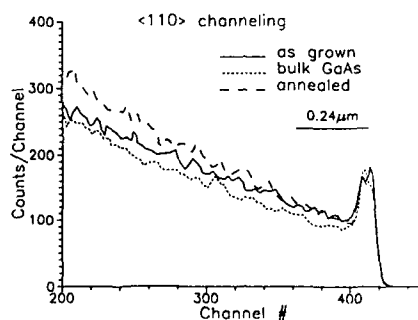


Fig. 2 1.95 MeV $\langle 110 \rangle$ aligned RBS spectra from a LTMBE layer ($T_g=200^\circ\text{C}$) as grown, annealed in As overpressure at 600°C , and a bulk GaAs standard.

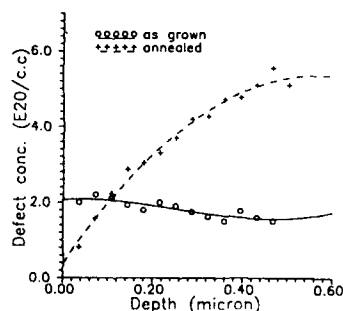


Fig. 3 Point defect concentration, n_D as a function of depth derived from the channeling spectra in Fig. 5 for the as grown and annealed LTMBE layer.

Table I. A summary of the average critical half angles, $\psi_{1/2}$, the minimum yield, χ_{\min} , and the x ratios obtained for the $\text{Ga}_{K\alpha}$ and $\text{As}_{K\beta}$ scans of the bulk GaAs standard and the as grown and annealed LTMBE GaAs layers.

	Average $\psi_{1/2} <110>$ ($\pm 0.03^\circ$)		$x = \frac{\psi_{1/2}(\text{Ga}_{K\alpha})}{\psi_{1/2}(\text{As}_{K\beta})}$	χ_{\min}	
	$\text{Ga}_{K\alpha}$	$\text{As}_{K\beta}$		$\text{Ga}_{K\alpha}$	$\text{As}_{K\beta}$
Bulk GaAs	0.79	0.85	0.93	0.20	0.17
As-grown LTMBE	0.78	0.74	1.05	0.23	0.22
Annealed LTMBE	0.78	0.80	0.97	0.21	0.20

and $\text{As}_{K\beta}$ scans and χ_{\min} for the bulk standard, the as-grown and the annealed LTMBE layers.

The ratios $x = \psi_{1/2}(\text{Ga})/\psi_{1/2}(\text{As})$ for the three samples are also tabulated.

In Table I we notice that $x=0.93$ for bulk GaAs, slightly lower than the calculated value 0.97. Since the ratio of the x-ray absorption coefficient of $\text{As}_{K\beta}$ to that of the $\text{Ga}_{K\alpha}$ in GaAs is ≈ 2 , the mean emission depth of the $\text{Ga}_{K\alpha}$ is greater than that of the $\text{As}_{K\beta}$. The net effect of this is that the $\psi_{1/2}(\text{Ga})$ becomes narrower due to dechanneling of the beam at greater depth in the sample. Therefore $x < 0.97$ in our measurement is consistent with the calculation. For the as-grown LTMBE layer, $x=1.05$, much greater than that for bulk GaAs. Notice also that the absolute values of the $\psi_{1/2}(\text{Ga})$ for the three samples are equal within a measurement error ($\pm 0.04^\circ$). The significant narrowing of the $\psi_{1/2}(\text{As})$ for the as grown LTMBE layer indicates that the $<110>$ channel as defined by the As strings is smaller. The most probable cause for this is the presence of As atoms slightly displaced from the normal As position into the $<110>$ channel. Since the PIXE results reveal that $\approx 4 \times 10^{20}$ excess As atoms/cm³ are present in the layer, the narrowing of the $\psi_{1/2}(\text{As})$ can be interpreted as the result of the presence of excess As atoms located close to the As atom rows.

In Fig. 4(b) we also observe two "kinks" in the $\text{As}_{K\beta}$ scan at tilt angle $\approx 0.35^\circ$ in both directions of the scan for the as-grown LTMBE GaAs as indicated by the arrows in the figure. It should be pointed out that although these "kinks" are only slightly larger than the measurement error, they are reproducible in the as-grown sample but are not observed in either the annealed or the bulk standard sample. However, due to the relatively large statistical error, the following quantitative analysis on these "kinks" can only provide a rough estimation. Using the continuum model formulated by Lindhard [14], the atomic displacement r_x can be related to the $\psi_{1/2}$ by the following expression:

$$\psi_{1/2} \propto \sqrt{\ln\left(\frac{C_a}{r_x} + 1\right)}$$

where C is a constant and a is the Thomas-Fermi screening distance. For a normal crystal, r_x is just the transverse rms thermal vibration amplitude, p (≈ 0.1202 Å for GaAs). A rough estimate using 0.35° as the half angle for the displaced As atoms yields a projected displacement $r_x \approx 0.3$ Å in the as-grown LTMBE sample.

In the $<110>$ axis, as the sample is tilted parallel to a $\{110\}$ plane, the ion beam will interact with an As string in one direction and a Ga string in the other direction. This asymmetric effect has been used to identify the lattice location of impurity atoms in many III-V semiconductors [15,16]. In our channeling results, the direction toward the negative tilt angles corresponds to the direction toward the As string. This is confirmed by the Rutherford

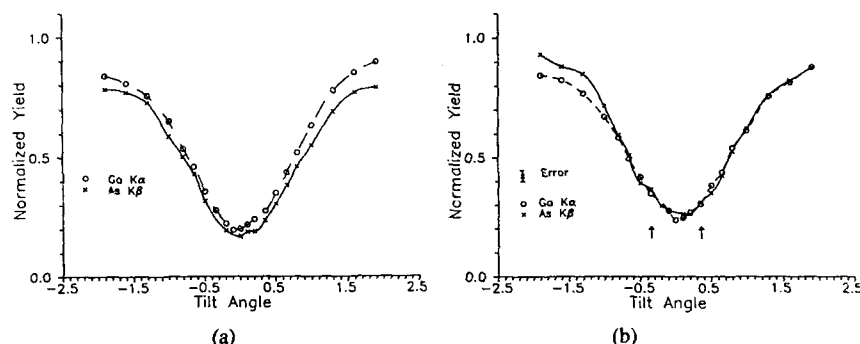


Fig.4 Angular scans of the $GaK\alpha$ and $AsK\beta$ x-rays obtained as the samples are tilted parallel a $\{110\}$ plane about a $\langle 110 \rangle$ axis for (a) a bulk GaAs standard, and (b) the LTMBE GaAs layer. Note the "kinks" in (b) in the As scan.

backscattering results recorded simultaneously with PIXE. The $\psi_{1/2}$'s and x ratios for $GaK\alpha$ and $AsK\beta$ from both the bulk and the as-grown LTMBE GaAs as the sample is tilted toward the As row parallel to a $\{110\}$ plane are tabulated in Table II. The pronounced narrowing in the $AsK\beta$ scan from the LTMBE GaAs sample suggests that the excess As atoms in the sample are preferentially bonded to the As atoms in the normal As sites. The stronger "kink" toward the As string direction in the As scan in Fig. 4(b) also confirms this suggestion.

Experiments performed on as-grown LTMBE-GaAs layers using convergent beam electron diffraction (CBED) and large-angle diffraction pattern (LACBED) [10] suggested that the excess As atoms in these layers do not reside on tetrahedral interstitial sites. The CBED and LACBED results can be explained by assuming that the As atoms form lower symmetry split interstitials along the $\langle 111 \rangle$ axis, i.e., assuming that an As atom at $1/4 \ 1/4 \ 1/4$ in the unit cell is shifted to a new position $1/8 \ 1/8 \ 1/8$ and an interstitial is inserted at $3/8 \ 3/8 \ 3/8$ [10]. Our PIXE/channeling results are compatible with this suggestion.

Ion channeling experiments on the annealed LTMBE sample show that the narrowing on the $AsK\beta$ scan is less than that of the as-grown sample. For the annealed sample, $x=0.97$, slightly higher than that of bulk GaAs. The slight narrowing of the $AsK\beta$ scan of this sample may then be caused by the random scattering from these As precipitates. The slight increase in the $\chi_{\min}(As)$ of this annealed sample as compared to the standard also indicates that $\sim 1-2\%$ of the As atoms in the sample are not in registry with the matrix as viewed along the $\langle 110 \rangle$ direction.

The PIXE/channeling results reveal that the excess As atoms in the as-grown LTMBE layer are not in exact interstitial positions but are sitting close to the normal As sites in the lattice. Therefore, the dechanneling factor σ_D [12] for these As atoms is expected to be smaller. With this adjustment in σ_D the calculated n_D from the RBS/channeling data is $\sim 2.5 \times 10^{20} \text{cm}^{-3}$ and is still lower than $\Delta[As]$ in the layer. The only explanation is that a fraction of these excess As atoms are in exact substitutional position not contributing to the dechanneling. Recently, using

Table II. A summary of the critical half angles, $\psi_{1/2}$, and the x ratios for the $GaK\alpha$ and $AsK\beta$ scans from the bulk GaAs standard and the LTMBE GaAs layer obtained when the samples are tilted toward the As atom string along a $\{110\}$ plane.

	$\psi_{1/2} \langle 110 \rangle$ toward the As row		x ratio
	$GaK\alpha$	$AsK\beta$	
Bulk GaAs	0.78	0.81	0.96
LTMBE GaAs	0.76	0.68	1.12

optical absorption and electron paramagnetic resonance techniques, Kaminska *et al.* [7] found $\sim 1.2\text{--}1.3 \times 10^{20} \text{ cm}^{-3}$ neutral As_{Ga} antisites in an as-grown LTMBE layer grown at $T_g = 200^\circ\text{C}$. This result is in good agreement with our observations on ion channeling.

CONCLUSIONS

We have found a high level of excess As, $\Delta[\text{As}] \approx 0.01$, in LTMBE GaAs layers grown at substrate temperature $\approx 200^\circ\text{C}$. The $\Delta[\text{As}]$ in the layer is believed to be responsible for the dilation of the lattice constant in the as-grown layers. Upon annealing in As atmosphere above 450°C these excess As coalesce forming As precipitates. A large fraction ($\sim 60\%$) of the excess As atoms in the as-grown layers are found to occupy a position very close to the normal As sites in the lattice. The rest of the excess As atoms are believed to be in As_{Ga} antisites.

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Surface Ordering of MBE Grown 001 $Ga_{1-x}Al_xAs$ - A Theoretical Study

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Abstract

The kinetics of MBE growth of $Ga_{1-x}Al_xAs$ is studied theoretically using the stochastic model of MBE growth based on the master equation approach and the random distribution approximation. The surface ordering phenomenon during the 001 growth of $Ga_{0.5}Al_{0.5}As$ is investigated as a function of the growth conditions. The atom pair interaction energy parameters for various surface configurations were obtained from the first principle calculations. The other model parameters needed in the description of the kinetic processes are obtained from the available experimental data. The ordering kinetics is studied as a function of fluxes, flux ratio and growth temperature. The degree of ordering is estimated in terms of the short range order parameter. The short range order parameter increases with temperature till 650°K and 750°K for cation to anion flux ratios 2 : 1 and 1 : 5, respectively. Beyond this critical temperature, the short range order parameter decreases. This critical temperature is identified as the kinetic order-disorder temperature. The order-disorder phenomenon observed in this theoretical study is explained in terms of the dependence of the surface migration rate of the cations on the growth temperature. The dependence on the order-disorder temperature on the flux ratio is attributed to decreased surface migration for larger flux ratios.

1 Introduction

Presence of long range ordering in the as grown epilayers reduces the band gap of the materials and thus has implications in the device applications. Long range order has been observed in many compound semiconductors grown by MBE and MOCVD [1-6]. A few of the compound semiconductors which exhibit long range order in as grown samples are: $GaAlAs$, $GaAsSb$, $InAsSb$, $GaInAs$ and $GaInAsP$. The presence of ordering in the epilayers is usually observed using transmission electron microscopy (TEM). The ordering observed in these compounds is shown to be growth and surface conditions and orientation dependent. For example, in MBE grown $Ga_{1-x}Al_xAs$, it was observed that the degree of ordering as observed in terms of the intensity of superstructure reflections in TEM observations, depends on the substrate orientation, growth temperature and the Al content. The epitaxial strain between substrate and the epilayer is also shown to play a role in deciding the type and degree of ordering [6].

In this manuscript, the stochastic model approach developed for the study of the MBE growth of compound semiconductors [9,10] is employed to study the MBE surface ordering kinetics in $Ga_{1-x}Al_xAs$. In section 2, a brief discussion of the stochastic model for the MBE alloying studies is presented. The results of the surface ordering kinetic study of $Ga_{1-x}Al_xAs$ along with a discussion of the results is presented in section 3. Conclusions of this study are stated in section 4.

2 Stochastic Model for Alloy Kinetic Studies

The details of the development of the stochastic model for the MBE growth of alloy compound semiconductors are presented elsewhere [9,10]. Due to limited space, only the salient features of the stochastic model are discussed in the following section.

2.1 Time Evolution Equations of MBE Kinetics

The stochastic model describes the time evolution of the macrovariables of growth in terms of rates of the surface kinetic processes. The development of the model is based on the master equation scheme and the random distribution approximation. A detailed discussion of the development of the stochastic model is given in Ref.[9,10]. The assumptions necessary for the derivation are: (i) a rigid zinc blende lattice oriented along 001 direction. (ii) effect of surface reconstruction and strain are neglected (iii) creation of anti site defects is excluded. The kinetic process used in the description of the time evolution equations are: adsorption, evaporation, and surface migration. The adsorption of atoms is assumed to be equal to the arrival rate if the cations arrive on the anion surface or the anion arrives on the cation surface and zero otherwise. In other words, the sticking probabilities for atoms arriving on proper surface is unity. The evaporation and surface migration processes are described in terms of Arrhenius type rate equations involving exponential prefactors and binding energies of the atoms. It is noted that there are two types of surface migration- intralayer and interlayer surface migrations. The general form of the rate equation for the evaporation and the surface migration processes is as follows:

$$R = \frac{1}{\tau} e^{E_{act}/kT} \quad (1)$$

where R is the rate of the kinetic process and the E_{act} is the activation energy for the kinetic process. The E_{act} for evaporation is the binding energy of the surface atom. E_{act} for the surface migration is always less than the energy of binding of the atom.

2.2 Macrovariables

Two sets of macrovariables - one for each sublattice can be defined. For the purpose of this study, we will assume that the cations, Ga and Al belong to the even sublattice and the anion, As , belongs to the odd sublattice. The macrovariables for the $2n^{th}$ layer are: concentration variables, $C_{Ga}(2n)$ and $C_{Al}(2n)$, atom-vacancy bond densities, $Q_{Ga}(2n)$ and $Q_{Al}(2n)$ and atom-atom bond densities, $\tilde{N}_{GaAl}(2n)$, $\tilde{N}_{GaGa}(2n)$ and $\tilde{N}_{AlAl}(2n)$. All the bonds referred in this manuscript are the second nearest neighbor bonds, when the whole crystal is considered. They are also the first nearest neighbor inplane bonds in the (001) plane. Of the seven macrovariables, only five are independent because of the following relations:

$$\tilde{N}_{GaGa}(2n) = 2 C_{Ga}(2n) - \frac{1}{2} Q_{Ga}(2n) - \frac{1}{2} \tilde{N}_{GaAl}(2n)$$

for $Ga - Ga$ bond density,

$$\tilde{N}_{AlAl}(2n) = 2 C_{Al}(2n) - \frac{1}{2} Q_{Al}(2n) - \frac{1}{2} \tilde{N}_{GaAl}(2n)$$

for $Al - Al$ bond density and

$$\tilde{N}_{vv}(2n) = 2(C_v(2n)) - \frac{1}{2}Q(2n) \quad (2)$$

where

$$C_v(2n) = (1.0 - C(2n))$$

and

$$C(2n) = C_{Ga}(2n) + C_{Al}(2n)$$

and

$$Q(2n) = Q_{Ga}(2n) + Q_{Al}(2n)$$

where $C_v(2n)$ is the vacancy density, and $C(2n)$ is the total atom concentration in the $2n^{th}$ layer. In Eqn (2), it is assumed that the inplane coordination number is four. Similar set of equations can be written for the anion sublattice. For the study $Ga_{1-x}Al_xAs$, only the cation sublattice is alloyed and therefore, there are two kinds of atoms- Ga and Al are present in the cation sublattice and only As atoms present in the anion sublattice. There will be five independent variables for the cation sublattice and two independent variables for the anion sublattice. Thus, there is a total of seven independent macrovariables whose time evolution needs to be modeled for a complete description of the MBE growth kinetics. In this study, the independent variables for the cation sublattice are chosen as: $C_{Ga}(2n)$, $C_{Al}(2n)$, $Q_{Ga}(2n)$, $Q_{Al}(2n)$ and $\tilde{N}_{GaAl}(2n)$. For the anion sublattice, the independent variables are: $C_{As}(2n+1)$ and $Q_{As}(2n+1)$.

2.3 The $Ga_{1-x}Al_xAs$ Alloy System and the Model Parameters

The alloy system studied is $Ga_{0.5}Al_{0.5}As$. The $Ga - Ga$ and $Al - Al$ second nearest neighbor pair interaction energies were obtained from the first principle calculations as [11]:

$$V_{Ga-Ga} = -0.096eV,$$

$$V_{Al-Al} = -0.096eV$$

and

$$V_{Ga-Al} = 0.096eV \quad (3)$$

It is noted that the $Ga - Al$ pair interaction energy is more positive than that of $Ga - Ga$ and $Al - Al$ suggesting that surface ordering can occur if the surface migration of atoms is high enough to allow atoms to sample a variety of surface configurations involving different combinations of cations as the nearest neighbors.

The model parameters employed in this study are obtained from the data available on the MBE growth of $GaAs$ described in Ref.[9,10]. The growth conditions considered for this study are: flux rate of cations is $2 \text{ \AA}/\text{sec}$; cation to anion flux ratio are 2 : 1 and 1 : 5; substrate temperature is in the range of $400 - 890^\circ\text{K}$. The relaxation time constants, τ_{rGa} , τ_{rAl} , τ_{rAs} , and the surface migration time constants, $\tau_d^{intraGa}$, $\tau_d^{intraAl}$, $\tau_d^{intraAs}$, $\tau_d^{interGa}$, $\tau_d^{interAl}$ and $\tau_d^{interAs}$ and flux parameters, L_{Ga} , L_{Al} , L_{As} were obtained by a similar procedure detailed elsewhere [9] and are reported in Table I for various growth conditions.

Since the equations governing the time evolution of the macrovariables are coupled nonlinear first order differential equations, they are not analytically integrable. They were numerically integrated using a predictor-corrector numerical integration scheme on a SUN Sparc station. The average computational time for a typical growth of 3-6 monlayers was 20 CPU hours.

Table I. Model parameters, the relaxation time constants, τ_{RGa} and τ_{RA_s} , the flux parameters, L_{Ga} and L_{A_s} , the interaction energy parameters, K_{Ga-Ga} and K_{Al-Ga} , and the surface migration parameters, τ_{DGA} and τ_{DA_s} as a function of growth temperature for flux ratio 2 : 1 and 1 : 5. It is noted that $\tau_{RGa} = \tau_{RAI}$; $L_{Ga} = L_{Al}$; $K_{Ga-Ga} = K_{Al-Al}$; $\tau_{DGA} = \tau_{DAI}$.

$T^\circ K$	τ_{RGa}	L_{Ga}	τ_{RA_s}	L_{A_s}	K_{Ga-Ga}	K_{Ga-Al}	K_{As-A_s}	τ_{DGA}	τ_{DA_s}
					Flux Ratio 2:1				
400	3.5E12	27.8	8.3E28	65.54	-1.78	1.78	9.42	45.82	6.9E10
450	4.1E09	21.1	1.5E24	54.58	-1.58	1.58	8.37	15.15	29.1E07
500	18.1E06	15.7	2.28E19	43.52	-1.42	1.42	7.54	1.011	3.58E06
550	21.6E03	11.2	1.7E17	38.65	-1.29	1.29	6.85	0.110	99.3E03
600	5.4E03	7.50	4.4E14	32.67	-1.18	1.18	6.28	0.017	5.0E03
650	236.7	4.41	2.8E12	27.61	-1.10	1.10	5.80	3.7E-03	3.9E2
700	16.27	1.74	3.7E10	23.28	-1.02	1.02	5.39	9.6E-04	4.6E1
725	4.91	0.54	5.3E09	21.6	-0.98	0.98	5.2	5.8E-04	17.35
775	0.56	-1.60	1.6E08	17.8	-0.92	0.92	4.9	1.8E-04	3.00
825	8.3E-04	-3.51	7.2E6	14.7	-0.87	0.87	14.8	6.9E-05	6.4E-01
890	9.7E-03	-5.72	2.2E5	11.3	-0.80	0.80	4.23	2.3E-05	1.1E-01
					Flux Ratio 1:5				
400	3.52E12	27.9	8.3E28	67.8	-1.78	1.78	9.42	446.82	6.870E10
550	21.64E03	11.2	1.7E17	41.0	-1.29	1.29	6.85	0.110	99.32E03
600	5.37E03	7.538	4.432E14	35.0	-1.18	1.18	6.28	0.017	5.008E03
700	16.27	1.739	3.70E10	25.6	-1.019	1.019	5.386	9.597E-04	45.760
750	1.6	-0.58	8.64E08	21.9	-0.95	0.95	5.03	3.0E-04	6.7
800	0.21	-2.61	32.3E06	18.6	-0.89	0.89	4.71	1.09E-04	1.35
890	9.68E-03	-5.69	2.21E05	13.6	-0.80	0.80	4.23	2.3E-05	1.1E-01

3 Results and Discussion

The macrovariables, $C_{Ga}(2n)$, $C_{Al}(2n)$, $C_{As}(2n+1)$, $Q_{Ga}(2n)$, $Q_{Al}(2n)$, $Q_{As}(2n+1)$, and $\dot{N}_{GaAl}(n)$ were obtained as a function of time for various temperatures in the range of 400-890°K. The short range order (SRO) parameter given by:

$$SRO = \frac{\sum_{i=1}^3 \left(\frac{\dot{N}_{GaGa}(2n) + \dot{N}_{AlAl}(2n) - \dot{N}_{GaAl}(n)}{C(2n)} \right)}{\sum_{i=1}^3 \left(\frac{\dot{N}_{GaGa}(2n) + \dot{N}_{AlAl}(2n) + \dot{N}_{GaAl}(2n)}{C(2n)} \right)} \quad (4)$$

was evaluated for various temperatures. The layers numbered 1 to 3 are the first three layers which are about 95% complete. Plot of SRO parameter versus temperature is shown in Figures 1a-b for flux ratios 2 : 1 and 1 : 5, respectively.

In the case of flux ratio 2 : 1, the SRO parameter increases till 650°K and then decreases with increasing temperature as shown in Figure 1a. In the case of flux ratio 1 : 5, the SRO parameter increases till 700°K, and then decreases with temperature as shown in Figure 1b. Thus, the temperature at which the SRO parameter starts to decrease, called the kinetic order-disorder temperature is found to be 650°K and 750°K for the flux ratios 2 : 1 and 1 : 5, respectively. The temperature dependence of the SRO parameter can be explained as follows. In the low temperature range, the surface migration is small and therefore, cations adsorb at the sites in and around the sites of their arrival. As the arrival of the atoms is random, they adsorb and incorporate on the lattice randomly

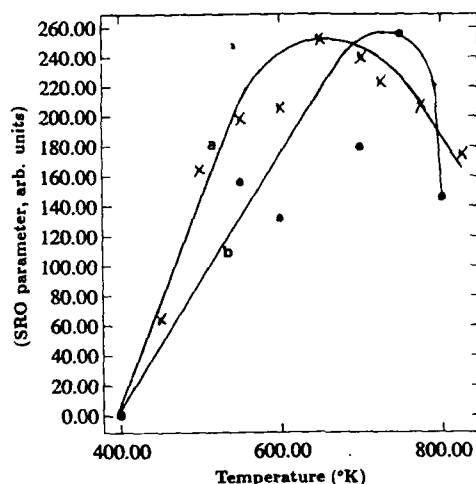


Figure 1. Plot of SRO parameter versus growth temperature for flux ratios (a) 2 : 1 and (b) 1 : 5.

which results in a complete random distribution of the $Ga - Ga$, $Al - Ga$ and $Al - Al$ surface bonds. Therefore, the SRO parameter is negligible. As the temperature increases, the surface migration rate increases resulting in more chances for the cations to sample various nearest neighbor configurations. In the process of sampling, the cations end up with the energetically most favorable nearest neighbor configurations which in this case are Ga having Al and Al having Ga as their nearest neighbors. Thus, as the temperature increases the SRO parameter increases. Beyond the order-disorder temperature, the SRO parameter decreases due to two kinetic effects. The thermal energy is large enough to break the stronger $Ga - Al$ bonds. Thus, the thermal randomization of the nearest neighbor bonds results in less ordering and a small SRO parameter. The other kinetic effect is due to the random evaporation of surface cations which randomizes the nearest neighbor bonds. The second kinetic effect is minor at the order-disorder temperature due to low thermal energy and becomes pronounced above $800^{\circ}K$.

The temperature dependence of the order-disorder temperature with flux ratio is explained as follows. As the flux ratio increases, the effective number of surface migration jumps of a cation decreases because the time interval between the time of its arrival on the surface to the time of adsorption of an anion on it, decreases. In other words, the effective length of time for which the cation is on the surface during which it is free to surface migrate decreases with flux ratio. Therefore, to achieve the same level of effective surface migration, extra thermal energy is needed for higher flux ratios. Therefore, the order-disorder temperature increases with the flux ratio. Influence of evaporation of the kinetics of order-disorder at temperatures close to the order-disorder temperature were found to be minor.

4 Conclusion

In this study, a theoretical model of MBE growth is employed to study the surface ordering kinetics of $Ga_{1-x}Al_xAs$ as a function of growth conditions. The degree of ordering was calculated in terms of the SRO parameter. It was observed that the SRO parameter increases with increasing temperature in the low temperature range and then decreases. The temperature of this transition from order to disorder called kinetic order-disorder

temperature is identified for flux ratios 2 : 1 and 1 : 5, as 650°K and 750°k. The kinetics of the surface ordering phenomenon as a function of growth condition is shown to be dependent of the effective surface migration of cations. It is also shown that beyond 800°K, the evaporation of cations dominates the kinetics.

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PART III

Applications of LT GaAs

ELECTRONIC AND OPTOELECTRONIC APPLICATIONS OF MATERIALS GROWN AT A LOW TEMPERATURE BY MBE

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ABSTRACT:

Materials grown at a low temperature by MBE and subsequently annealed at a high temperature have an excess amount of Arsenic and have demonstrated high dielectric breakdown strength and low carrier lifetime. These properties have found applications in analog and switching power applications, in picosecond pulse generation, in device isolation and in the selective intermixing of heterostructures. This paper reviews these applications.

1. INTRODUCTION:

Low Temperature GaAs or LT GaAs refers to GaAs grown at a low temperature (typically 200°C) by MBE. The material and its initial applications were pioneered by Calawa and Smith at the MIT Lincoln Laboratories. Their work concentrated on material that was grown at 200°C and subsequently annealed at 600°C for 10 minutes. This stabilized LT GaAs was found to be highly resistive and optically inactive. These properties have been exploited in a variety of electronic and opto-electronic applications which this paper will attempt to review.

2. ELECTRONIC APPLICATIONS:

2.1 LT Materials as a Buffer.

The first application of LT GaAs by Smith et al[1], was as a buffer for a GaAs MESFET. The most dramatic impact as shown in figure 1 was on the virtual elimination of backgating in these MESFETs compared to those fabricated on proton implanted undoped buffers. Sidegating is caused by the injection of carriers from a contact which modify the depletion region at the substrate/channel interface and hence the channel current[2]. This current is suppressed by orders of magnitude by LT GaAs because the large trap density in the material ($>10^{19}\text{cm}^{-3}$) raises the trap-filled limit voltage, V_{TFL} , before the onset of charge injection.

LT buffer technology has also been applied to the AlInAs-GaInAs HEMT system. Brown et al[3], compared the performance of HEMTs with LT AlInAs

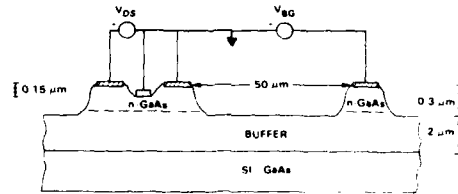
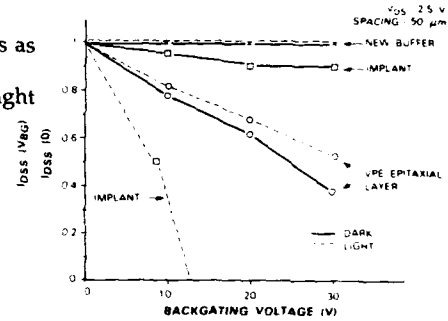
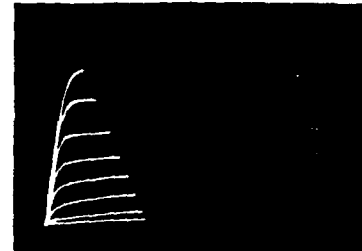


Figure 1: Experimental data from Smithetal[1] verifying that LT GaAs as a buffer virtually eliminated backgating in the dark and in the light compared to conventional buffers.



Ga _{0.47} In _{0.53} As	CONTACT	$5 \times 10^{18} \text{ cm}^{-3}$	70 Å, 30 Å
Al _{0.48} In _{0.52} As	SCHOTTKY		315 Å, 150 Å
Al _{0.48} In _{0.52} As	DONOR DOSE	$4 \times 10^{12} \text{ cm}^{-2}$	50 Å, 0 Å
Al _{0.48} In _{0.52} As	SPACER		15 Å
Ga _{0.47} In _{0.53} As	CHANNEL		360 Å
AlInAs/GaInAs	SUPERLATTICE		360 Å
Al _{0.48} In _{0.52} As	BUFFER	$T_{\text{growth}} 200^{\circ}\text{C}, 150^{\circ}\text{C}$ SAMPLES 2319, 2397	2250 Å
InP:Fe SUBSTRATE			

Figure 2: The epitaxial layer design and the performance of AlInAs/GaInAs HEMTs with 0.2 μm gate length. The kink effect is effectively suppressed in these devices[3].



(grown at 150°C and subsequently annealed at 500°C for 10 minutes) and conventional AlInAs buffers. As shown in figure 2, the LT AlInAs buffer eliminated the kink in the I-V characteristic which occurs in AlInAs-GaInAs HEMTs with conventional buffers. The kink is considered to be caused by the field ionization of traps in the AlInAs buffer. The change in trap occupancy shifts the threshold voltage of the device and hence the drain current. The LT AlInAs provides a very high density of traps with a very high capture and emission rate which renders the trap occupancy and hence the threshold voltage independent of the electric field, eliminating the kink effect. Record power-delay product of 4fJ per gate[4], was obtained from ring oscillators fabricated using HEMTs with the LT AlInAs buffer.

2.2 LT GaAs as a Gate Insulator.

The major issue in power MESFETs is the breakdown voltage of the gate-drain diode. Figure 3 illustrates schematically the four regions where breakdown can occur i.e. (1) the bulk, (2) the surface, (3) the drain and the (4) the channel/substrate interface. All of these are regions of local electric field maxima. Models provided by Barton and Ladbroke[5], Mizuta et al[6] and Trew and Mishra[7] suggest that under most operating conditions, surface leakage and breakdown explains the details of observed MESFET breakdown behavior. Yin et al[8] utilized the high breakdown strength of a surface layer of LT GaAs placed under the gate to delay the onset of surface breakdown. As shown in figure 4, this resulted in the doubling of the gate-drain breakdown voltage over a conventional MESFET. Figure 4 also illustrates that an AlAs layer was used as a barrier between the LT GaAs and the underlying channel to prevent the back diffusion of As from the LT GaAs into the channel. Chen et al[9] fabricated MISFETs using a similar technology and obtained a record power output of 1.57W/mm at 1.1 GHz.

2.3 LT Materials as Diffusion Barriers.

The diffusivity of dopant species such as Be and Si in ternaries such as GaInAs and AlInAs is a strong function of growth temperature. The reduced diffusivity at low temperatures has been used by Metzger et al[10] and Schmitz et al[11] to good effect in improving the performance of AlInAs-GaInAs HBTs and HEMTs respectively. Figure 5 summarizes the device improvements achieved by introducing a LT GaInAs layer grown at 300°C as a diffusion barrier between the heavily doped p⁺GaInAs base and the n-AlInAs emitter. In the absence of the LT layer the Be diffuses into the AlInAs emitter locating the p-n junction completely within the AlInAs, hence forming a homojunction AlInAs emitter reducing β . Maintaining the integrity of the n-AlInAs/p-GaInAs heterojunction via the LT GaInAs spacer has resulted in devices with record f_T of 130 GHz and divider operation at 36 GHz.

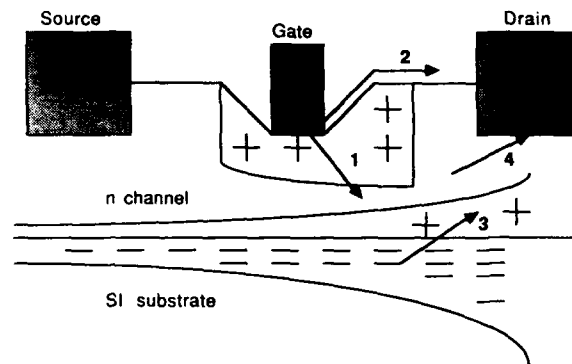


Figure 3: Schematic of an n-channel GaAs MESFET illustrating the four regions where breakdown can occur.

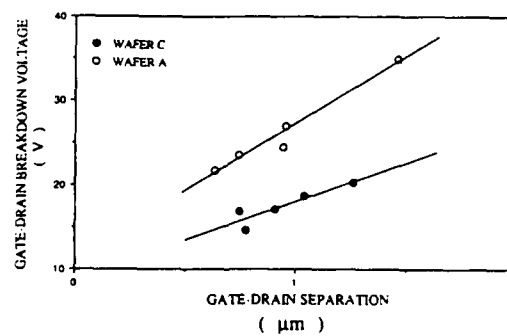
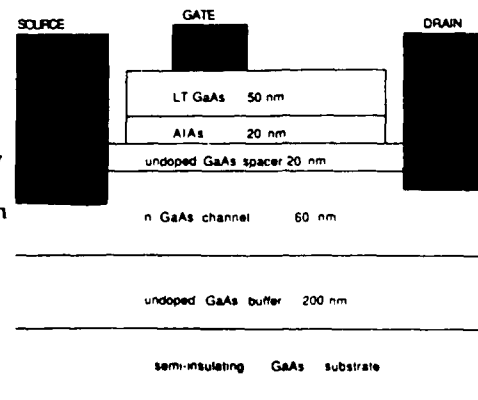


Figure 4: Using a LT GaAs surface layer separated from the channel by an AlAs diffusion barrier raises the breakdown voltage of the gate-drain diode compared to conventional MESFETs[8].



LT AlInAs has been used as an effective diffusion barrier in the case of inverted AlInAs-GaInAs HEMTs as shown in figure 6. The most difficult problem in this technology is that Si tends to surface segregate on AlInAs and dope the GaInAs channel leading to reduced electron mobilities. The introduction of a LT AlInAs spacer between the donor layer and the GaInAs channel traps the Si and prevents its incorporation in the channel. This has led to inverted modulation doped structures with sheet charge density, n_s , of $3 \times 10^{12} \text{cm}^{-2}$ and electron mobility of $10,000 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Devices with $0.2 \mu\text{m}$ gate length fabricated on this material yielded an f_T of 100 GHz and an f_{max} of 170 GHz.

2.4 LT Materials for Inter Device Isolation (LT GaAs based "LOCOS" process)

The tremendous advance in integration density in Si ICs has been primarily due to the availability of an oxide to achieve inter-device isolation e.g. by the LOCOS process. LT GaAs allows us to possibly mimic this process by substituting LT GaAs for the SiO_2 . The process flow as implemented is shown in figure 7. A dielectric sandwich of $\text{SiN}/\text{SiO}_2/\text{SiN}$ was first deposited on GaAs. A window was etched into this dielectric stack using a plasma of CF_4/O_2 . Next, the SiO_2 was preferentially undercut in BOE providing a dielectric profile suitable for lift-off. Next the GaAs is etched through the window in the dielectric and LT GaAs grown in the recess. The LT GaAs deposited on the dielectric is then lifted-off by etching away the dielectric. The process results in LT GaAs deposited locally separating active regions of the wafer much like SiO_2 does in a LOCOS process.

3. OPTOELECTRONIC APPLICATIONS OF LT GaAs

The opto-electronic applications of LT GaAs are derived from three main properties of the material

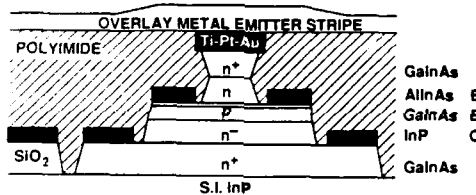
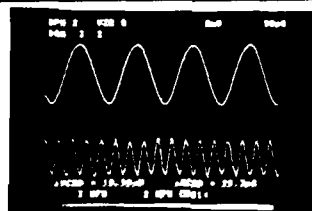
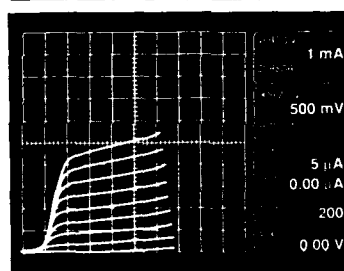
- (i) The high trap density in the material leads to very fast recombination times - a source of sub-picosecond pulses.
- (ii) The extremely low conductivity of the material provides inter-device isolation, and
- (iii) The excess As in the material is a source of As and its related defects.

In this section the three applications related to these properties will be presented.

3.1 Pico-second Pulse Generation using LT GaAs.

A convenient way to generate pico-second pulses is by generating a short circuit in a transmission line through electron-hole pair generation via Q-switched laser illumination. Figure 8 illustrates the approach of Frankel et al [12] which is typical for this technique. The rise time and fall time of the

DHFT CROSS SECTION

COMMON EMITTER I-V ($2 \times 5 \mu\text{m}^2$)

34 GHz DIVIDER WAVEFORM

Figure 5: Using a LT GaInAs spacer (the thin insert in the base), suppresses Be diffusion and improves device performance. Though a 34 GHz waveform is shown, a maximum divider frequency of 36 GHz was achieved.[10]

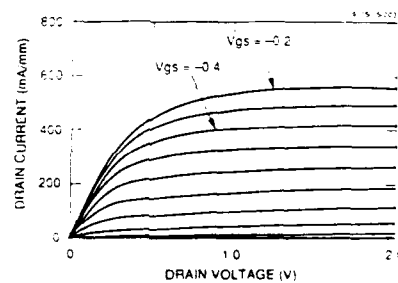
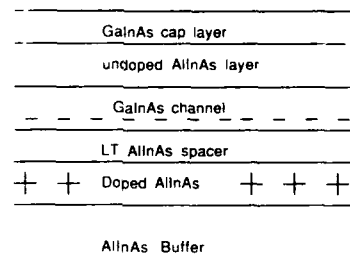


Figure 6: Using a LT AlInAs spacer suppresses surface segregation of Si in AlInAs preventing incorporation in the GaInAs channel and improving channel mobility in inverted HEMTs.

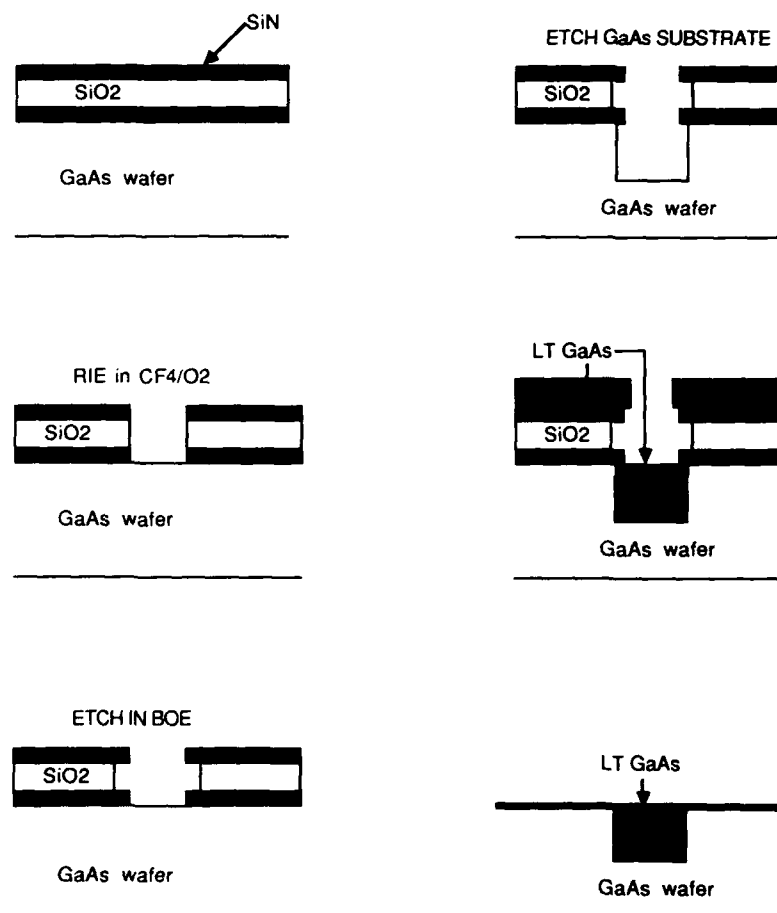


Figure 7: Process flow for implementing selective deposition of LT GaAs to achieve inter-device isolation. The compound semiconductor analog of LOCOS.

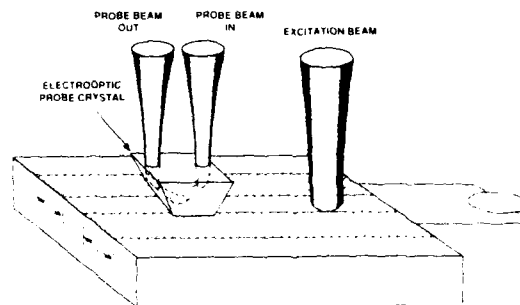


Figure 8: Geometry of experimental coplanar picosecond switches[12] and the observed radiation burst[13].

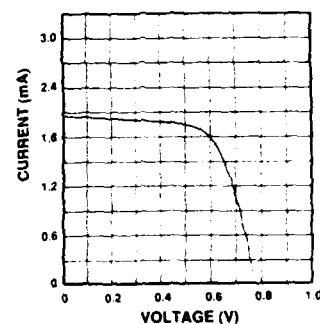
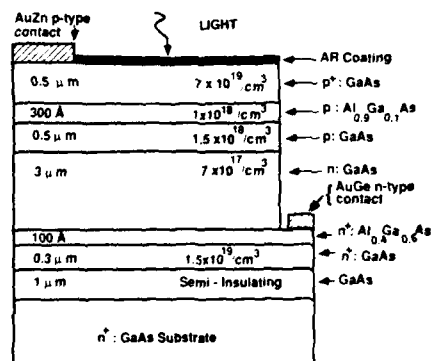
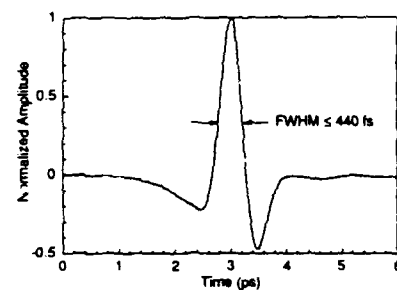


Figure 9: The epitaxial layer design and performance of a solar cell fabricated on an LT GaAs buffer[14].

voltage transient is determined by the electron mobility and recombination time of the material respectively. The materials of choice until the development of LT GaAs had been proton implanted Si or GaAs. The implant damage reduced the electron lifetime but also reduced the electron mobility increasing the rise time while reducing the fall time of the pulse. LT GaAs, however, has adequate electron mobility while still having a large trap density and low recombination lifetime. These two properties together along with the high dielectric breakdown strength of the material leads to large pulses with extremely fast responses. Chwalek et al[13] have demonstrated a FWHM of 440fs using LT GaAs grown at 190°C with an associated radiated spectrum beyond 2.5THz.

3.2 LT GaAs as Epitaxial Isolation Layers in Solar Cells.

Efficient integration of solar cells to provide large output power requires either current matching or voltage matching. Subramaniam et al[14] utilized LT GaAs between component cells to achieve electrical isolation, which could be achieved previously with only hybrid mechanically stacked structures. The structure of the AlGaAs/GaAs photovoltaic cell with epitaxial isolation as fabricated is shown in figure and its photovoltaic response in figure 9. The low efficiency of the cell of 5.4% is primarily due to the low fill factor caused by the series resistance of the n-type contact layer. This problem can be readily solved by increasing the carrier concentration and thickness of the layer. This technology enables the integration of subcells that absorb different portions of the solar spectrum onto a single substrate increasing not only the output power but also the power conversion efficiency.

3.3 Picosecond Photoconductivity using LT GaAs

To get picosecond response from photoconductors it is necessary to reduce the lifetime of the photoconductive material. This requires damaging the semiconductor which in turn affects the electron transport properties. The reduced electron velocity results in a reduced electron transit time and hence a long photoconductive response. Morse et al[14] alleviated this problem by using a graded AlGaAs layer grown above a LT GaAs layer as shown in figure 10. Here the electrodes for the photoconductor are placed on the graded AlGaAs region which serves as the transport layer. The built in field in the AlGaAs is directed towards the underlying LT GaAs layer. The photogenerated carriers drift in the AlGaAs and are collected by the electrodes. When the incident radiation is switched off the electron-hole pairs drift towards the underlying LT GaAs layer where they recombine. The peak output current was increased by a factor of six and the responsivity by a factor of ten compared to conventional photodetectors.

3.4 Influence of LT GaAs on the Interdiffusion of GaAs/AlGaAs Heterostructures

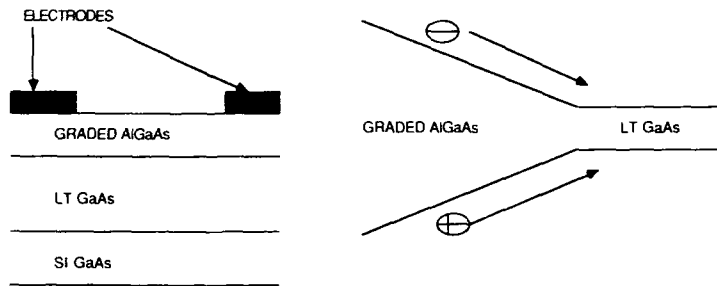


Figure 10: Picosecond photoconductivity obtained by having separate high quality graded AlGaAs drift layers and LT GaAs recombination layer[15].

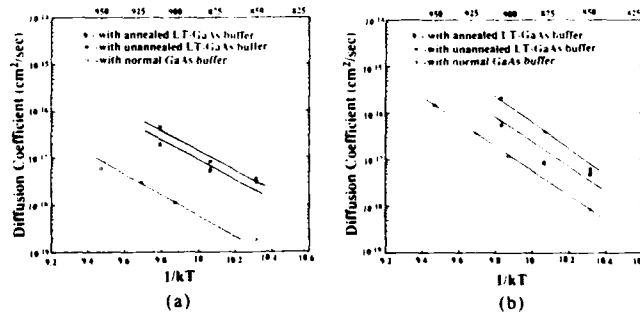
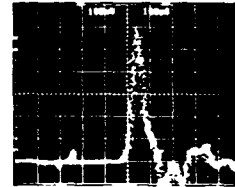


Figure 11: The interdiffusion coefficient of the Group III elements obtained from the photoluminescence shift of AlGaAs-GaAs quantum wells grown on LT GaAs buffers under (a) Ga and (b) As overpressure.

An unique use of LT GaAs layers was investigated by Hwang et al where the excess As and its related defects (such as Ga vacancies) in the LT GaAs layer was used to intermix AlGaAs/GaAs heterostructures. Intermixing of heterostructures is in prevalent use to provide lateral optical confinement in lasers. Here the selective conversion of a superlattice into a random alloy increases its bandgap and hence provides the lateral confinement. The disordering is conventionally achieved via defects generated while selectively diffusing dopants such as Si and Zn through the structures using SiN as a mask. A single AlGaAs-GaAs quantum well was grown on an LT GaAs buffer and the interdiffusion coefficient of the group III elements was determined by the change in the photoluminescence characteristic of the quantum well. Assuming an error function composition profile, the states of the quantum well were calculated using Schrodinger's equation and fit to the observed emission wavelength. Figure 11 shows the diffusion coefficient extracted from the PL data. The buffers investigated were an unannealed LT GaAs buffer, an annealed LT GaAs buffer and a normal GaAs buffer.

This technology may find applications in integrated opto-electronics.

4. Conclusions:

The progress in the applications of LT GaAs in both electronics and optoelectronics has been rapid. Since the first use of this material as a buffer in 1988, it has found use in power MESFETs, picosecond pulse generation, high voltage high speed switches, picosecond photodetectors, solar cells and integrated optoelectronics. The sensational pace of progress and the increase in the number of researchers in this field promises to provide an increasing number of exciting applications in the future.

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MATERIAL AND DEVICE CHARACTERISTICS OF MBE MICROWAVE POWER FETs WITH BUFFER LAYERS GROWN AT LOW TEMPERATURE (300°C)

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ABSTRACT

MBE GaAs grown at low temperature (300°C) is evaluated for its suitability as a buffer layer for microwave power FETs. Hall effect and capacitance-voltage (C-V) measurements show that low temperature (LT) buffers may have strong deleterious effects on the electronic quality of FET active layers unless they are heat-treated in-situ at 600°C and topped with a thin (~0.1µm) 600°C GaAs buffer prior to growth of the FET active layer. The voltage isolation properties of the LT buffers are found to be thermally stable to rapid thermal anneals up to 870°C for 10 seconds.

Transmission electron microscopy (TEM) cross-sections were examined on FET layers with LT buffer layers which ranged in thickness from 0.1µm to 1.0µm. The TEM reveals a high density (~10¹⁷ cm⁻³) of small (<100Å) arsenic precipitates in all of the buffer layers studied. In cases where the LT buffer is not heat treated and topped with a thin 600°C GaAs buffer layer, dislocations and arsenic precipitates extend from the buffer layer into the FET active layer. Their presence in the active layer correlates with the degradation in electronic properties observed with Hall effect and C-V. Microwave power FETs were measured at DC and 5 GHz. DC and RF results for devices with LT buffer layers are comparable to devices with conventional buffer layers.

INTRODUCTION

It has been known since the 1970s that MBE GaAs grown at temperatures below ~450°C and rates of ~1µm/h exhibits semi-insulating behavior, [1,2] but only recently has the mechanism for this behavior begun to be investigated in detail and seriously examined for potential applications such as field effect transistors [3,5] and optoelectronic detectors.[6] The LT buffer layer has been demonstrated to be useful for the reduction of sidegating or backgating for FETs [3] and HEMTs, [5] though not without some degradation in the performance of digital circuits.[5]

In this work we compare materials and device characteristics of microwave power FETs grown by MBE on LT and conventional buffer layers. Hall effect and capacitance-voltage (C-V) measurements are utilized to qualify the electronic quality of the FET active layers grown on top of LT buffers, and to guide the development of growth procedures for FET structures on LT buffers. Transmission electron microscopy (TEM) measurements are used to evaluate the microstructural defects in the epitaxial layers. DC and RF power measurements are reported for 5 GHz power FETs grown on conventional and LT buffer layers.

MATERIAL GROWTH AND MEASUREMENTS

More than twenty growth runs were made in two different Varian GEN II MBE systems. GaAs (100) undoped substrates prepared by the LEC method were used exclusively. Substrates were solvent cleaned, chemically etched in 5:1:1 (H₂SO₄ : H₂O₂ : H₂O), and rinsed in DI water prior to introduction in the MBE system. In the system, the substrates were heated to 600°C in an As₄ flux

to desorb the surface oxide, as verified by reflection electron diffraction. GaAs growth was then commenced at 300°C with a V/III beam equivalent pressure ratio of ~ 15 and a growth rate of $\sim 1\mu\text{m/h}$, except for the control wafers where growth was initiated and maintained at 600°C. The thickness of the LT buffer layers and post-growth steps (whether or not they were heat treated in-situ at 600°C in an As_4 flux, or capped with a thin 600°C buffer before growth of the active layer) were varied to achieve electronic quality in the doped active layer comparable to the control wafers with conventional buffer layers. The active layer was silicon-doped. A representative epitaxial test layer structure is shown in Figure 1.

The electronic quality of the doped active layers was assessed with Hall effect (van de Pauw) at 300K and electrolytic C-V profiling. The voltage isolation properties of the buffer were assessed with a mesa-to-mesa current-voltage characteristic on a test structure such as depicted in Figure 2. Voltage breakdown was defined at a current of $10\mu\text{A}$ and was abrupt in all cases. The structural quality was assessed with TEM. TEM measurements were performed on cross-sectional samples using bright field imaging. $1.0\mu\text{m}$ gate length microwave power FETs were fabricated using the standard GE C-band (5 GHz) MMIC process. This particular process has a large database of results from VPE and MBE-grown devices, both of which behave similarly. VPE and MBE control wafers were processed in the same lot with the LT buffered wafers.

CHARACTERIZATION RESULTS

A. Electrical Measurements

Table I shows the wafer growth and characterization data for five wafers. Wafer No. 1176 is a control wafer, with a conventional MBE undoped buffer grown at 600°C. This yields a breakdown voltage of 40 Volts for our standard breakdown voltage test structure at a current of $10\mu\text{A}$ (Figure 2). Breakdown was abrupt on all of the wafers, but substantially higher (250 Volts) for the low temperature buffers. The Hall effect and C-V results show considerably more active layer back-side depletion for low temperature buffers.

Comparing No. 1176, the control wafer, with No. 1180, which has an LT buffer which was untreated before growth of the active layer, we observe a 33% reduction in total free electrons with Hall effect. Comparing No. 1176 and 1177, which has an LT buffer which was heat treated at 600°C after growth, we observe a 24% reduction in total free electrons. If we heat treat the LT buffer at 600°C and then cap it with a $0.1\mu\text{m}$ 600°C buffer as in No. 1181 and illustrated in Figure 1, then we observe no significant free electron reduction (1%) or electron mobility reduction (2%) from the control wafer. The trend indicates that with a suitable combination of heat treatment and cap buffer

300nm	GaAs Active Layer	Silicon doped ($n = 3 \times 10^{17} \text{ cm}^{-3}$)
100nm	GaAs 600°C Buffer Cap	Undoped
1 μm	GaAs Low Temperature (300°C) Buffer Layer	Undoped
	LEC GaAs Substrate Undoped	

Figure 1. MBE Low Temperature Buffer Layer Test Structure

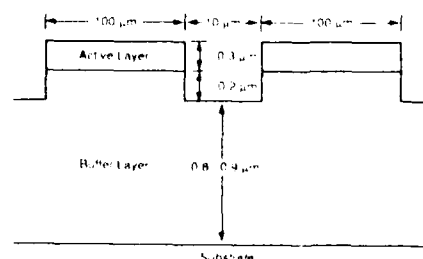


Figure 2. Mesa Pattern for Buffer Layer Breakdown Voltage Test. Mesas are $100\mu\text{m} \times 100\mu\text{m}$ squares.

Table I. MBE Low Temperature Buffer Results (1 μm LT Buffer Thickness)

WAFER No.	GROWTH DATA				CHARACTERIZATION DATA			
	BUFFER GROWTH TEMP.	600°C HEAT TREATMENT TIME	600°C CAP BUFFER THICKNESS	BREAKDOWN VOLTAGE	HALL EFFECT (300K)		C-V	
					SHEET DENSITY (10^{12} cm^{-2})	MOBILITY ($\text{cm}^2/\text{V-s}$)	PROFILE THICKNESS	
1176	600°C	None	None	40V	8.52	3800	Flat	0.31 μm
1177	300°C	20 min.	None	250V	6.40	3510	Sloped	0.25 μm
1180	300°C	None	None	260V	5.66	3640	Sloped	0.25 μm
1181	300°C	20 min.	0.1 μm	250V	8.42	3670	Flat	0.30 μm
1182	300°C	None	0.1 μm	250V	7.39	3630	Flat	0.29 μm

thickness, the active layer electrical properties can be equivalent to those grown on normal MBE buffers, and that the high voltage breakdown can be preserved.

The C-V data is also very revealing, showing a substrate with a thinner active layer for No. 1177 and 1180 (0.25 μm) and a sloped carrier profile. For example, Figure 3 compares 1176 and 1177. The sloped profile indicates that the added depletion by low temperature buffers is due to more than simply a difference in Fermi levels between the active layer and low temperature buffer, and may partially be due to some grown-in defects in the active layer. TEM measurements described below

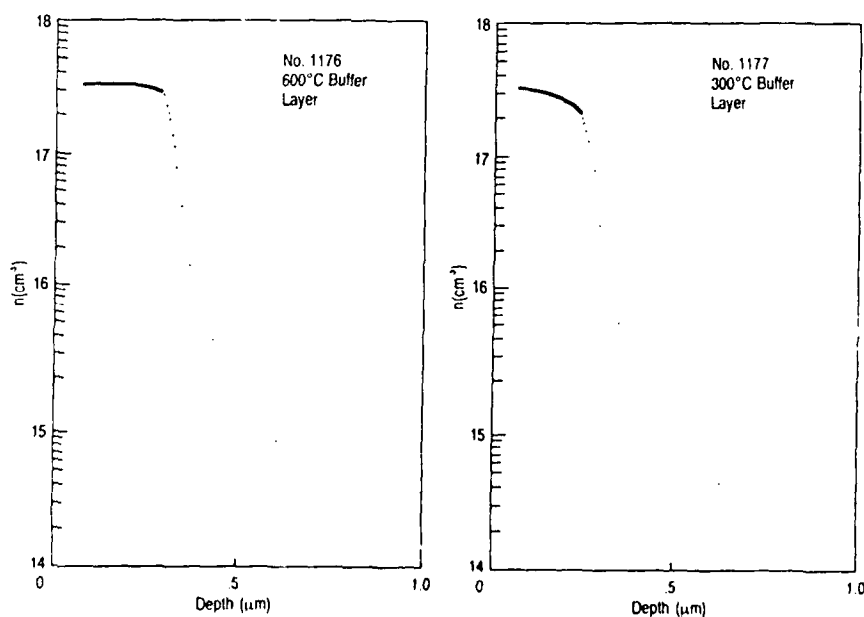


Figure 3. Electrolytic Capacitance-Voltage Profiles of MBE FET Structures Shown in Figure 1. (a) conventional 600°C MBE buffer layer, wafer No. 1176, (b) low temperature buffer layer heat treated at 600°C for 20 minutes before growth of silicon-doped active layer, wafer No. 1177. Profile of No. 1177 is sloped and shallower than the control wafer, indicating the presence of grown-in defects.

clearly show the presence of dislocations and, in some cases, arsenic precipitates extending from the LT buffer into the active layer. The C-V data resembles the data for conventional buffers when the LT buffer is heat treated and capped with a thin 600°C buffer. Thus, C-V and Hall effect results are consistent.

Thinner low temperature buffers (0.1-0.5 μm thick) with variable heat treatment times (5-20 min.) and 0.1 μm cap buffers were also investigated. Thinner buffers are desirable because they promote lower densities and smaller sizes of oval defects, as well as a shorter growth time. LT buffers of 0.4, 0.25, and 0.1 μm (wafers 1185, 1186, 1187) all exhibited good Hall data and C-V profiles. Data is summarized in Table II. The 0.4 μm buffer had a breakdown voltage of 190V while the thinner layers both had a 160V breakdown voltage. With thinner buffer layers, the test measures the breakdown voltage of the substrate (typically 160V) plus the voltage dropped across the LT buffer because the mesa height is comparable to the epitaxial layer thickness.

The 600°C in-situ heat treatment of the LT buffer was investigated to determine if the time could be shortened. A shorter time would obviously enhance wafer throughput. Layers with 0.1 μm LT buffers capped with 600°C 0.1 μm layers were grown with LT buffer heat treatment times of 20, 15, 5, 0 minutes (wafers 1187, 1188, 1189, 1195). The layers that were heat treated all exhibited 160V breakdowns and good C-V profiles. Hall data indicated a slight improvement with a five minute versus a 15 or 20-minute heat treatment. Reduced impurity incorporation on account of the reduced time may be a factor for further consideration. The layer (1195) with no heat treatment exhibited a poor C-V profile (sloped and reduced thickness) and reduced Hall effect free electron sheet density. We find that a five minute heat treatment of the LT buffer is sufficient and possibly better than the 20 minute heat treatment.

To investigate the effects of a high impurity background, a wafer (1196) was grown with the LT buffer intentionally doped with Si at a level of $3 \times 10^{17} \text{ cm}^{-3}$. The breakdown was unaffected by this doping. This indicates that the LT buffer will be highly tolerant to wide variations of background impurities in epitaxial systems, and so will likely enhance the repeatability of buffer insulating properties, and possibly enhance MMIC yield.

Wafers 1176, 1180, 1177, and 1181 were subjected to rapid thermal annealing (RTA) to study the effects of high temperature anneals used to remove implant damage for n⁺ ohmic layer formation. A piece of each wafer was used for four different anneal cycles, then C-V measurements were made. Anneal cycle #4 is used for implant ohmic formation. Data is summarized in Table III. Results of the RTA study show that the only LT buffer structure that behaved as well as the standard buffer was the LT buffer which was heat treated in-situ before being capped with a 600°C buffer, consistent with

Table II. MBE Low Temperature Buffer Results (Varying LT Buffer Thickness)

WAFER NO.	GROWTH DATA				BREAKDOWN VOLTAGE	CHARACTERIZATION DATA			
	BUFFER GROWTH TEMP.	LT BUFFER THICKNESS	600°C HEAT TREATMENT TIME	600°C CAP BUFFER THICKNESS		HALL EFFECT (300K)		C-V	
						SHEET DENSITY (10^{12} cm^{-2})	MOBILITY ($\text{cm}^2/\text{V-s}$)	PROFILE THICKNESS	
1185	300°C	0.4 μm	20 min.	0.1 μm	190V	9.85	3590	Flat	0.29 μm
1186	300°C	0.25 μm	20 min.	0.1 μm	160V	10.7	3580	Flat	0.31 μm
1187	300°C	0.1 μm	20 min.	0.1 μm	160V	9.62	3550	Flat	0.29 μm
1188	300°C	0.1 μm	15 min.	0.1 μm	160V	9.61	3530	Flat	0.29 μm
1189	300°C	0.1 μm	5 min.	0.1 μm	160V	10.0	3630	Flat	0.29 μm
1195	300°C	0.1 μm	None	0.1 μm	185V	8.03	3610	Sloped	0.27 μm
1196	300°C	0.5 μm	20 min.	None	185V	6.84	3460	Sloped	0.25 μm

earlier comments. Mesa isolation measurements were also performed on layers 1176, 1177, 1180, and 1181 after anneal cycle #4. The voltage breakdown dropped ~10V on the LT samples and was unchanged on the control wafer, showing that the isolation properties are stable to RTA anneals.

B. TEM Measurements

All images were taken in the bright field mode on or near the $\langle 110 \rangle$ pole. Figure 4(a) is a cross-sectional micrograph of No. 1177. Small ($<100\text{\AA}$) particles are clearly visible in the LT buffer layer, while the substrate and Si-doped active layer grown at 600°C are apparently free of particles. Figure 4(b) is a TEM micrograph taken at higher magnification near the center of an LT buffer layer. Moire fringes, which result when two crystals of different lattice parameter overlap, are clearly seen in many of the particles. Since the fringes are often in the same direction and have the same spacing, it may be concluded that the particles are crystalline and many have a similar orientation with respect to the GaAs matrix. Particle densities are on the order of 10^{17}cm^{-3} . High resolution imaging is shown in Figure 5. A separation of 2.8\AA was measured for the most strongly diffracting planes in the particles. This compares well with the most prominent d-spacing in rhombohedral arsenic, which is due to the $\{102\}$ planes at 2.77\AA .

Similar TEM observations of arsenic precipitates in LT GaAs were reported recently in LT GaAs samples which were heat-treated in-situ after growth [7, 8] and LT GaAs samples which were used as buffer layers for subsequent HEMT layer growth.[9, 10] TEM comparisons between as-grown LT GaAs and heat-treated LT GaAs indicates that arsenic incorporates interstitially in as-grown LT GaAs, and that precipitates form during subsequent heat treatment of continued layer growth at higher temperatures [7, 8].

For buffer layers studied here, typical precipitate diameters range from 20 to 50\AA , with a somewhat higher density and larger size near the center of the LT buffer. For sample 1180, which was not heat treated prior to growth of the Si-doped layer, arsenic precipitates are clearly visible in

Table III. Effects of Rapid Thermal Annealing Cycles on C-V Active Layer Profiles Grown on LT Buffers.

LAYER	CYCLE #1	CYCLE #2	CYCLE #3	CYCLE #4
1176 Conventional Buffer + Active	No Change	No Change	No Change	Slight drop in doping. Slightly rounded interface. Increased surface depletion.
1180 LT + Active	No Change	Increased Sloping. Rounded Interface.	Flatter profile due to increased surface depletion.	Drop in doping. Flatter profile due to Increased surface depletion. Rounded interface.
1177 LT + Heat Treatment + Active	No Change	Rounded Interface	Same as above	Much increased surface depletion.
1181 LT + Heat Treatment + Cap + Active	No Change	No Change	No Change	Slight drop in doping. Slightly rounded interface. Increased surface depletion.

Anneal Cycle #1— $400^\circ\text{C}/10$ second + $600^\circ\text{C}/10$ second

Anneal Cycle #2— $400^\circ\text{C}/10$ second + $700^\circ\text{C}/10$ second

Anneal Cycle #3— $400^\circ\text{C}/10$ second + $800^\circ\text{C}/10$ second

Anneal Cycle #4— $400^\circ\text{C}/10$ second + $650^\circ\text{C}/10$ second + $870^\circ\text{C}/10$ second

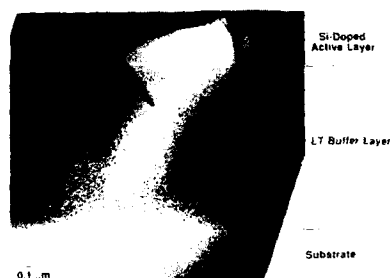


Figure 4A

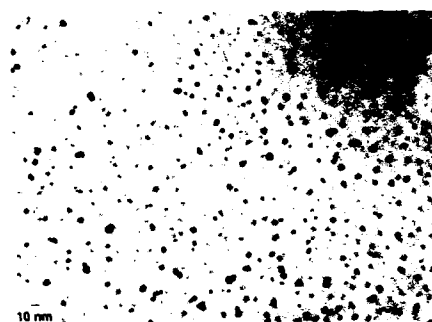


Figure 4B

Figure 4. (a) Cross-Sectional (110) Bright Field TEM Image of Wafer No. 1177 Showing Arsenic Precipitates Confined to the Low Temperature Buffer Layer. Dislocations extend from the LT buffer into the silicon-doped active layer. Dislocations were not observed in samples with LT buffers which were both heat treated at 600°C and capped with a 0.1μm 600°C buffer. (b) Cross-sectional (110) bright field TEM image of arsenic precipitates near the center of an LT buffer. Moire fringes indicate that many of the precipitates are similarly oriented with respect to the GaAs matrix.

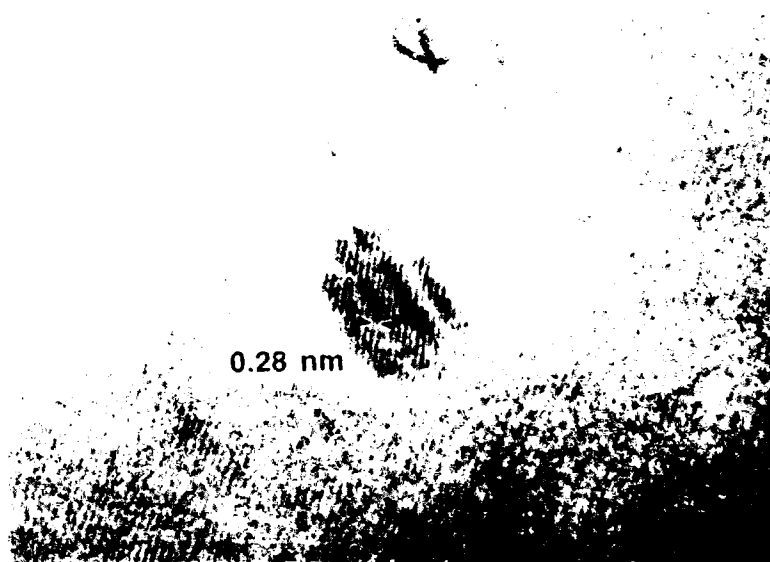


Figure 5. High resolution (110) Bright Field TEM Image of crystalline arsenic precipitate. 2.8Å separation compares well with the most prominent d-spacing for rhombohedral arsenic.

the active layer near the LT buffer interface. It is plausible that arsenic interstitials near the top and bottom of the LT buffer can diffuse out of the LT buffer during the 600°C heat treatment or subsequent layer growth. This could explain differences in 1177 and 1180. During the 20 minute heat treatment for 1177, arsenic interstitials in the near surface region can diffuse to the surface and desorb, leaving the near surface region with a lower density of arsenic precipitates. For 1180, which has no heat treatment, the interstitials can diffuse into the active layer during growth and form precipitates in the active layer.

Also seen in Figure 4(a) are dislocations which appear to originate near the center of the LT buffer layer and extend up into the Si-doped layer. Dislocations were not observed in cross-sections of samples 1182 (1.0µm LT buffer) or 1195 (0.1µm LT buffer), though on that basis we cannot rule out their presence because plan view imaging over large areas was not performed. The LT buffers in both of these were not heat treated, but were capped with 0.1µm 600°C buffers, and both showed some degradation in the electronic properties of their active layers, but not as much as 1177 or 1180. This indicates that a 600°C capping buffer layer is more important than heat treatment. LT buffers which were not heat-treated, but were capped with relatively thick (1.0µm) 600°C layers were shown to yield modulation-doped structures with comparable characteristics to structures grown on conventional buffers.[4, 9].

C. Device Measurements

FETs were fabricated in the same process run on MBE-grown layers with and without an LT buffer. The LT buffers were 0.9µm-thick, grown at 300°C, heat treated at 600°C in an As₄ flux for 20 minutes, and then capped with a 0.1µm 600°C buffer. The conventional buffers were 1.0µm-thick, grown at 600°C. A small number of sample FETs were tested for DC and RF characteristics. Power characteristics were obtained at 5 GHz with manual tuning.

The FETs were processed with the standard GE 1µm power MMIC process. The doping profile consists of a 0.2µm, highly doped cap layer and a 0.5µm active layer with $1 \times 10^{17} \text{cm}^{-3}$ silicon doping. Ohmic contacts are made to the n⁺ cap layer using Ni/AuGe/Ag/Au metal that is subsequently annealed. The 1.2µm gate is located in a double recess structure. The first etch is used to remove the cap layer in the gate area and to ensure that the proper amount of doped material is present for subsequent process steps. The gate recess is formed using the same resist opening as for the gate itself. A conventional lift-off resist profile is used, resulting in a trapezoidal gate and in a recess significantly wider than the gate itself.

DC characteristics of conventional and LT-buffered devices, shown in Figure 6, are quite similar. Differences between peak currents, transconductances, and pinch-off voltages are all less than the differences that are normally encountered due to process variations. Backgating characteristics were superior for the LT-buffered devices, though this is not a strong consideration for MMICs since the devices are widely separated and the isolation provided by normal buffers is adequate.

A power saturation curve of the LT-buffered FET is shown in Figure 7. At similar drain bias points, the LT-buffered FET produces 0.41 W/mm and 6.7 dB gain while the FET with a conventional buffer produces approximately 0.49 W/mm with 7.4 dB gain. Power-added-efficiencies are essentially the same for the two devices. While the FET with a normal buffer shows significantly greater small signal gain, our experience shows that process variations are more likely to be the cause of the difference than material variations. The similarities in the saturation characteristics and in the drain current as a function of RF power (not shown) indicate that there are no significant differences in trapping or confinement mechanisms between the two buffers.

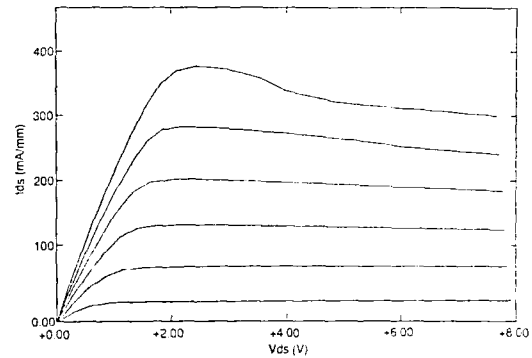


Figure 6A

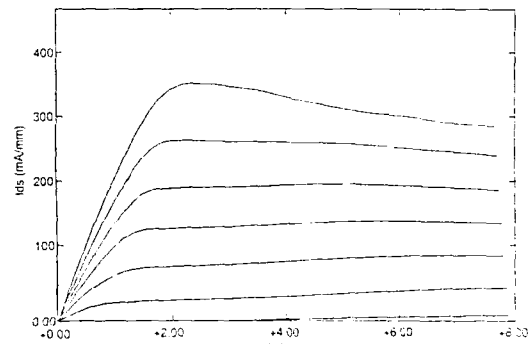


Figure 6B

Figure 6. I-V characteristics for 1x428 micrometer FETs (a) low temperature buffer, (b) conventional buffer. The gates are biased at 0.5 volts for the top curves with 1 volt steps between curves.

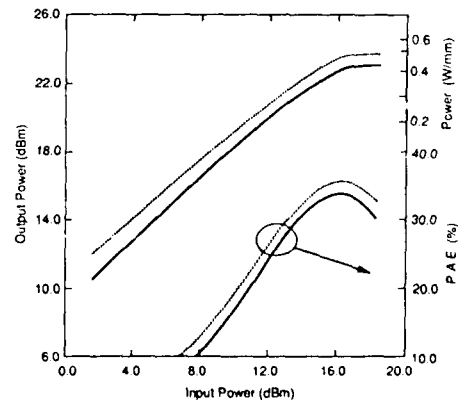


Figure 7. 5 GHz power saturation characteristics for the 1x428 micrometer FETs. Solid lines: FET with a low temperature buffer; dashed lines: FET with a conventional buffer. Drain biases were approximately 9.7 volts, and gate biases were optimized for high efficiency operation.

SUMMARY

Hall effect and C-V results on FET active layers show that LT buffer layers may have strong deleterious effects on the electronic quality of FET active layers unless the LT buffers are heat treated in-situ at 600°C and topped with a thin (0.1 μm) 600°C GaAs buffer prior to growth of the FET active layer. Dislocations and arsenic precipitates are observed to extend into the FET active layer in instances where the FET active layer is grown directly on an LT buffer which is not heat-treated, correlating with the degradation in electronic properties. DC and RF device measurements for microwave power FETs show comparable results for devices with conventional and LT buffers, and indicate no significant differences in trapping or confinement mechanisms between the two buffers.

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STUDY OF MODULATION IN GaAs MISFETs WITH LT-GaAs AS A GATE INSULATOR

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ABSTRACT

DC characteristics of a GaAs MISFET structure using low-temperature GaAs (LT-GaAs) as the gate insulator were investigated. MISFETs with different gate to channel separation (d) were fabricated. The dependence of four important device parameters such as gate-drain breakdown voltage (V_{BR}), channel current at zero gate bias (I_{DSS}), transconductance (g_m), and gate-drain turn-on voltage (V_{ON}) on the gate insulator thickness were analyzed. It was observed that (a) in terms of I_{DSS} and g_m , the LT-GaAs gate insulator behaves like an undoped regular GaAs layer and (b) in terms of V_{BR} and V_{ON} , the LT-GaAs gate insulator behaves as a trap dominated layer.

INTRODUCTION

Low temperature gallium arsenide (LT GaAs), grown by molecular beam epitaxy (MBE) at a low substrate temperature around 200°C [1], has recently attracted a lot of attention. It has been shown by many groups [1-4] that LT GaAs behaves quite differently depending upon growth condition (i.e. substrate temperature, V/III ratio, post growth anneal) ranging from being highly resistive ($>10^6 \Omega\text{-cm}$) to being conductive ($\sim 10 \Omega\text{-cm}$). *In-situ* postgrowth annealing of LT GaAs, grown at 200°C, for 10 minutes at 580°C, has been shown to result in a highly resistive and optically inactive insulating layers possibly due to approximately 1~2 at. % excess arsenic [1] and a large amount of antisite defects. When it is used as a buffer layer for GaAs metal-semiconductor field effect transistors (MESFETs), LT GaAs has largely eliminated sidegating (or backgating) effects and substantially reduced the output conductance [1]. When it is used as a gate insulator layer for GaAs metal-insulator-semiconductor field effect transistors (MISFETs), LT GaAs has significantly enhanced the breakdown voltage between the gate and the drain without sacrificing the channel current [2] and also greatly increased the output power density [3]. However, unannealed-LT GaAs has been shown to be very conductive due to hopping mechanism [4] through a deep level defect band. Obviously, unannealed-LT GaAs material will not be suitable as a buffer layer in MESFETs or as a gate insulator layer in MISFETs.

There is a fundamental difference between the thickness of LT GaAs as a buffer layer in MESFETs and as a gate insulator layer in MISFETs. While the former is typically up to 2 μm thick, the gate insulator layer needs to be as thin as possible (500Å~2000Å) to optimize device characteristics such as transconductance, etc. In this work we investigate the dependence of four important MISFET parameters such as transconductance (g_m), channel current at zero gate bias (I_{DSS}), the gate-drain breakdown voltage (V_{BR}), and the gate-drain turn-on voltage (V_{ON}) on the thickness of LT-GaAs gate insulator.

FABRICATION PROCESS

The device structures used for this experiment are shown in Figure 1. Four different MISFETs with (1) 4000 Å, (2) 2800 Å, (3) 1400 Å of LT-GaAs gate insulator, and (4) no LT-GaAs gate insulator were fabricated. The separation between gate and drain was typically 2 μm . Devices with gate length of 1.2 μm and gate width of 150 μm were tested.

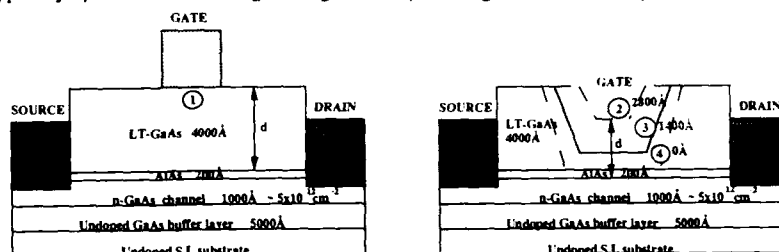


Figure 1. Device structures with four LT-GaAs recess depths

- (1) No LT-GaAs recess; LT-GaAs=4000 Å (2) LT-GaAs recess to 2800 Å
(3) LT-GaAs recess to 1400 Å (4) Recess to channel; LT-GaAs=0 Å

The sample was grown in a Varian Gen.II MBE system at a substrate temperature of 200°C and *in-situ* post annealed at 600°C for 10 minutes. The V/III equivalent beam pressure ratio was 12. The sample was under As over-pressure for temperatures above 500°C. During the temperature ramp up and down between 200°C and 500°C, the arsenic and gallium shutters were closed. Both the arsenic and the gallium shutters were opened at 200°C, and as soon as the growth of LT-GaAs layer was finished, both the arsenic and the gallium shutters were closed at the same time. The epitaxial structure consisted of a 5000 Å undoped GaAs buffer layer followed by a 1000 Å thick n-channel, both were first grown at 600°C. Then, a 200 Å AlAs layer and a 4000 Å thick LT-GaAs gate insulator were grown on the n-channel at 640°C and 200°C respectively. The sheet charge and carrier mobility, determined by Hall effect measurement, was $5 \times 10^{12} \text{ cm}^{-2}$ and $2500 \text{ cm}^2/\text{V}\cdot\text{sec}$.

The AlAs layer has proved [2,5] to be crucial in preventing undesired compensation of the underlying Si-doped n-channel as a result of the diffusion of excess arsenic from the LT-GaAs insulator. The AlAs layer also served as an etch stop for the LT GaAs etchant. Since the *in-situ* annealed LT-GaAs material is highly resistive, a low resistance ohmic contact to the n-doped channel through this layer is difficult to achieve. Therefore, before the AuGeNi-based metal evaporation, the LT-GaAs insulator must be selectively etched. It was found that the citric acid based chemical solution has highly etching selectivity between LT-GaAs and AlAs.

The device processing started with isolation formation by boron implantation, since a mesa structure etched by conventional wet chemical etching would result in the reduction of the gate-drain turn-on voltage (V_{on}) due to overlap of gate to n-channel over the mesa edges. Wet chemical etching of source and drain windows was shown to be not suitable due to excessive undercut in the device with 4000 Å thick of LT-GaAs gate insulator. Therefore, chlorine based reactive ion etching was used, followed by selective citric acid based wet chemical treatment. Then, the AlAs layer was removed by buffered HF before the AuGeNi-based metal evaporated. Finally, the LT-GaAs gate insulator recess was also done by using citric acid based chemical wet etching.

RESULTS AND DISCUSSION

The dependence of transconductance (g_m) on thickness of LT-GaAs gate insulator in $1.2 \times 150 \mu\text{m}$ MISFET devices was shown in Figure 2. The linear proportional relation of g_m on LT-GaAs gate insulator thickness demonstrated that the LT-GaAs layer behaved like an undoped GaAs layer, due to

$$g_m \approx \frac{C_{gs} v_s}{L_g} \quad (1)$$

where C_{gs} is the capacitance between gate and source, v_s is the carriers saturation velocity, and L_g is the gate length. As the LT-GaAs gate insulator thickness increases, the C_{gs} decreases, and so does the g_m .

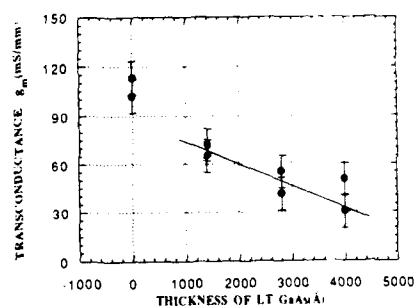


Figure 2. Transconductance vs LT-GaAs gate insulator thickness in $1.2 \times 150 \mu\text{m}$ MISFET.

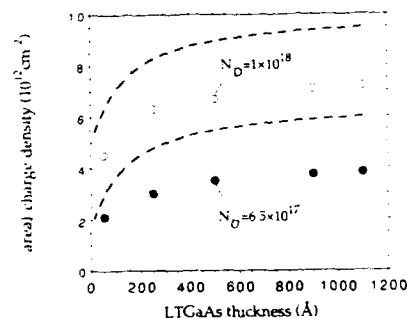


Figure 3. VDP measurements of channel depletion vs LT-GaAs thicknesses.
• Dashed line--calculated.
• White/black dots--measured.

In terms of undoped LT GaAs thickness (d), which was grown on the top of n-GaAs channel, the voltage dropped across the undoped LT GaAs and n-channel can be expressed as:

$$V = \frac{q N_D X_d^2}{2\epsilon} + \frac{q N_D X_d d}{\epsilon} \quad (2)$$

where X_d is the depletion depth, and N_D is the doping concentration in the channel. The calculated sheet charge versus undoped GaAs thickness was shown as the dashed line in Figure 3. The measured sheet charges, using the Van Der Pauw technique, with different LT-GaAs insulator thicknesses achieved by recess etching is also shown as the dots in Figure 3. Figure 4 shows the plot of I_{dss} of the $1.2 \times 150 \mu\text{m}$ MISFETs versus LT-GaAs insulator thicknesses indicating similar behavior as described by the above relationship providing further evidence that the LT-GaAs layer behaved as an undoped GaAs layer.

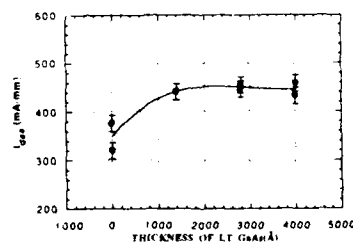


Figure 4. I_{dss} vs LT-GaAs gate insulator thickness in $1.2 \times 150 \mu\text{m}$ MISFET.

A turn-on voltages as high as 16 V was achieved for a MISFETs with 4000Å thick LT-GaAs gate insulator as shown in Figure 5. It exceeds the expected turn-on voltage of a Schottky gate on n-GaAs grown at normal substrate temperature by more than an order of magnitude. These high turn-on voltages, also observed by other groups [3], indicates that the dominant transport mechanism through the annealed LT-GaAs is space-charge-limited current (SCLC)[6]. The turn-on voltage is the same as trap-filled-limited voltage, V_{TFL} , defined as the voltage which corresponds to a sharp rise of current when all the traps were filled. It is found that experimental data does not obey the simple parabolic dependence of V_{TFL} on thickness derived from single, uniform trap theory given by [7]

$$V_{TFL} \approx \frac{q P_{t0} d^2}{\epsilon_s \epsilon_0} \quad (3)$$

where P_{t0} is the concentration of traps not occupied by electrons, d is the thickness of LT-GaAs insulator, q is the electronic charge, ϵ_s is the dielectric constant, and ϵ_0 is the permittivity of free space. This could be due to either a spatial variation in the trap density from a peak near the AlAs-LT GaAs interface to a minimum near the surface or due to the presence of several different trap levels[8]. Therefore, the characteristics of turn-on voltage (V_{on}) in MISFETs indicated that the LT-GaAs layer acted as a trap dominated layer.

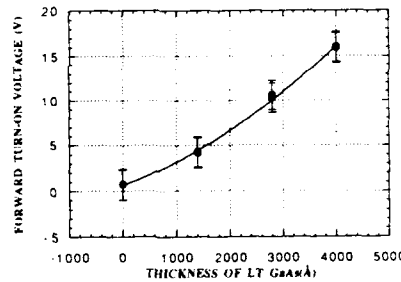


Figure 5. Turn-on voltage vs LT-GaAs gate insulator thickness in 1.2x150µm MISFET.

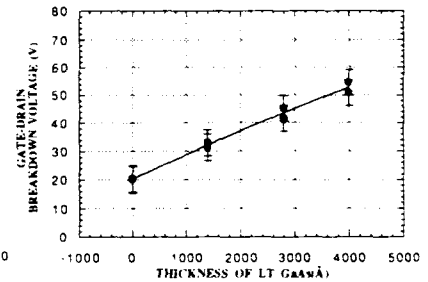


Figure 6. Gate-drain breakdown voltage vs LT-GaAs gate insulator thickness in 1.2x150µm MISFET.

The linearly dependence of the gate-drain breakdown voltages on the recessed LT-GaAs gate insulator thicknesses, as shown in Figure 6, also indicates that the LT-GaAs layer acted like a trap dominated layer in terms of gate-drain breakdown voltage (V_{BR}). We obtained the highest reported gate-drain breakdown voltage of 56 V with I_{dss} of 450mA/mm for a 1.2 x 150µm MISFET, as shown in Figure 7. The current-voltage characteristics of MISFETs as shown in Figure 8 demonstrated that the MISFETs behaved well even with 4000Å thick of LT-GaAs gate insulator. The high knee voltages of current-voltage characteristics was due to

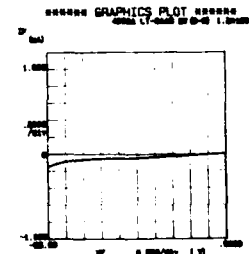


Figure 7. Gate-drain breakdown voltage with 4000Å thick LT-GaAs gate insulator in 1.2x150 µm MISFET.

higher ohmic contact resistance ($\sim 0.4-0.6 \Omega\text{-mm}$), since the source-drain area (i.e. same as n-channel) was only doped at $n_s \equiv 5 \times 10^{12} \text{cm}^{-2}$.

CONCLUSION

It is concluded that the characteristics of transconductance (g_m) and channel current at zero gate bias (I_{DSS}) indicates that the LT-GaAs insulator in a MISFET behaves like an undoped GaAs layer (grown at high substrate temperature). But, in terms of forward turn-on voltage and the gate-drain breakdown voltage, the LT-GaAs gate insulator acted as a trap dominated layer in a MISFET. It is, therefore, obvious that the optimization of LT-GaAs gate insulator thickness in a MISFET involves trade-off between different device parameters such as transconductance, gate-drain breakdown voltage and other parameters.

ACKNOWLEDGEMENTS

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STUDY OF TRANSPORT THROUGH LOW-TEMPERATURE GaAs SURFACE INSULATOR LAYERS

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INTRODUCTION

Since epilayers of GaAs grown at low substrate temperature (LTGaAs) and annealed at 600°C were first demonstrated to be an effective buffer layer for eliminating backgating effects, the material properties and electronic characteristics of bulk LTTGaAs have been actively investigated¹⁻³. Less attention has been paid to thin layers of LTTGaAs (~2000Å), although these have been shown to improve gate-to-drain breakdown characteristics when incorporated as the surface insulator layer in GaAs MISFET's⁴. In bulk LTTGaAs that has been annealed for 10 minutes at 600°C, the formation of arsenic precipitates with a density of 10^{18} cm^{-3} has been observed. These are considered to be at least partially responsible for the high resistivity of LTTGaAs². While the exact mechanism of precipitate formation is currently unknown, it would seem reasonable to expect the availability of the growth surface to have a significant effect on any defect redistribution during the anneal. This surface effect would become increasingly apparent as the LTTGaAs layer thickness was decreased. It is desirable for MISFET applications that the LTTGaAs gate insulator layer be as thin as possible, whilst maintaining high breakdown, in order to maximize device transconductance⁵. To achieve this, it is important to understand how the observed bulk features (such as ~60Å size arsenic precipitates) are affected in thin LTTGaAs layers.

In this work, we report on the investigation of current transport through 1000Å-5000Å thick LTTGaAs surface layers on an n-type GaAs channel. Room temperature I-V characteristics of schottky diodes incorporating a LTTGaAs surface layer are presented. The current mechanism through the LTTGaAs is found to be space-charge limited due to the high density of deep traps present. Comparison of the measured trap-filled limit voltage for different thicknesses of LTTGaAs suggests that the trap spatial distribution is non-uniform with respect to the growth direction, with a significant reduction in the trap density close (<1500Å) to the surface.

GROWTH STRUCTURE

The sample structure basically consists of a schottky diode, as shown in figure 1. The sample was grown by conventional MBE in a Varian Gen II, using solid source effusion cells. Important details of the growth are included below. The tetramer As_4 was used for all samples. Prior to LTGaAs deposition the substrate temperature (T_{sub}) was lowered from 600°C to 500°C in an As_4 flux. The As cell valve was then closed and T_{sub} lowered to the desired growth temperature. The temperature was measured by a thermocouple. For low temperature growth, the group III and group V source shutters were opened and closed simultaneously. The V:III beam equivalent pressure ratio was 16:1 throughout the growth.

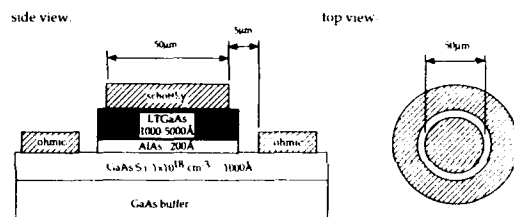


Fig. 1: MBE growth structure and diode processing structure. LTGaAs layer is grown at $T_{\text{sub}} < 400^\circ\text{C}$ on top of n-type channel grown at 600°C . AlAs layer grown at 600°C is included to prevent back diffusion of defects into the channel. Growth is interrupted during temperature ramp down.

After completion of the LTGaAs layer, the substrate temperature was raised to 500°C before the arsenic cell was reopened. The samples were then annealed for 10 minutes at 600°C in an arsenic overpressure. Unless otherwise noted, the LTGaAs was grown at 250°C . A 200Å thick AlAs layer grown at 600°C was always included between the n-type highly doped ($1 \times 10^{18} \text{cm}^{-3}$) GaAs channel and the LTGaAs surface layer to prevent excess arsenic incorporated at low temperatures from backdiffusing into the channel during the anneal⁴. Circular geometry diodes were processed on the samples, in which ohmic contacts were alloyed to the channel directly by etching through the LTGaAs. A Ti/Au schottky contact was deposited on the LTGaAs, and will be referred to below as the "gate". The gate-to-cathode separation is $5\mu\text{m}$. In this configuration, current flow is forced through the LTGaAs layer.

RESULTS AND DISCUSSION

Measured room temperature I-V curves for two samples are shown in figure 2. The LTGaAs surface layer was 2500Å thick for both, but the LTGaAs growth temperatures were 250°C and 400°C , as indicated on the graph. The 400°C sample exhibits "normal" schottky diode I-V characteristics, with a turn-on voltage of

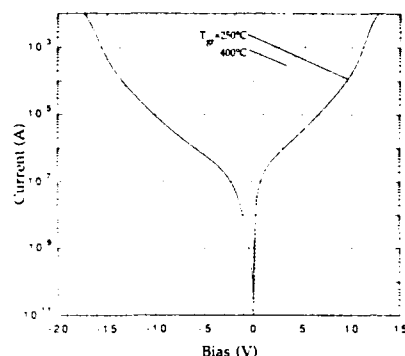


Fig. 2: I-V data for two diodes with 2500Å thick LTGaAs surface layer grown at 250°C (solid) and 400°C (dashed). Semi-log scale is used to show more detail. Note the similarity between forward and reverse bias for the 250°C sample. This is due to space-charge-limited current flow through the LTGaAs layer in the presence of traps.

around 0.8 V, and a reverse breakdown of around 10 V. The latter is high primarily because of the 2500Å of material between the gate and the channel. Indeed, there is essentially no difference between this sample and a control (not shown) in which 2500Å of intrinsic GaAs grown at 600°C replaces the LTGaAs surface layer. However, for the sample with LTGaAs grown at 250°C, the I-V characteristics of the diode have changed significantly. Most striking, is the similarity of forward and reverse bias current. Under forward bias, we observe an initial steep rise in the current with applied bias (0-0.2 V) followed by a shallow rise (1-10 V). Considering that the size of the diodes is 50μm in diameter, a current density of only 1 mA/mm² is observed under a forward bias of 5 V.

This result is easily understood if we consider the zero bias band diagram for our structure, which more closely resembles that of an M-I-S structure, rather than a schottky diode (figure 3). This is one reason why LTGaAs is often referred to as an insulator despite the fact that it is not a wide band gap material. This band diagram is inferred from the observed depletion of the underlying channel in Hall effect measurements by Van der Pauw technique⁶. The current mechanism for such a structure containing an insulator layer is typically space

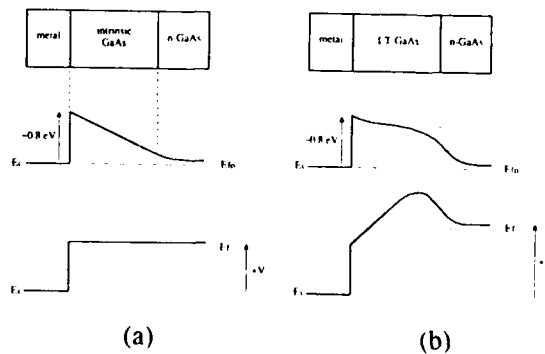


Fig. 3: Approximate Conduction band diagrams for normal schottky diode (a) and diode incorporating LTGaAs layer (b) under zero bias and forward applied bias conditions. Note the barrier to electron flow exists for the LTGaAs case even under large applied bias due to the presence of traps in the LTGaAs layer.

charge limited current (SCLC)⁷. This simply implies that an applied forward bias, V , does not directly correspond to raising the fermi-level eV towards the conduction band edge in the LTGaAs, as would be the case for a schottky diode with an intrinsic surface cap grown at 600°C. Neither does the surface layer act like a true dielectric. Instead, some or most of the applied bias is accommodated by space charge (band-bending) in the LTGaAs (see figure 3). Indeed, we observe such behaviour in our diodes, as shown in the I-V data by the low current levels under large forward bias.

The total space charge in the LTGaAs has contributions from the injected free carriers and the occupied traps. If the traps and free carriers are in local quasi-thermal equilibrium then the current, is limited by the traps since the quasi-fermi level in the LTGaAs cannot be raised by much more than kT above the trap energy level unless the traps are correspondingly filled (for a more detailed discussion the reader is referred to references 6 and 7).

A useful quantity in such a system is the so-called trap-filled limit voltage, V_{tfl} , which is defined as the voltage at which there is an abrupt, large change in the slope observed on a log-log plot of the I-V data. Physically, this roughly corresponds to the voltage required to fill all the traps in the insulator. For a single trap with a specific energy level and uniformly distributed, the temperature dependence of V_{tfl} yields the trap density and energy level⁷. Even in this case where there are known to exist several trap levels with a non-uniform spatial distribution the easily measured quantity V_{tfl} remains a qualitative indication of the average trap density in the insulator.

Since we were concerned with the effects on the excess arsenic related defects near the surface during the post-growth anneal, V_{tfl} were compared for two sets of diodes. In one series, diodes were processed on a sample grown with a 5000Å LTGaAs surface layer. After the anneal, the LTGaAs layer was etched back by different amounts prior to deposition of the gate metal. In the other series, samples with different thicknesses of LTGaAs were grown. Results for diodes with the same net insulator thickness were then compared. This is shown schematically in figure 4. The pertinent difference for the two cases is the relative accessibility of the growth surface to the trapped excess arsenic in the net LTGaAs layer, during the anneal.

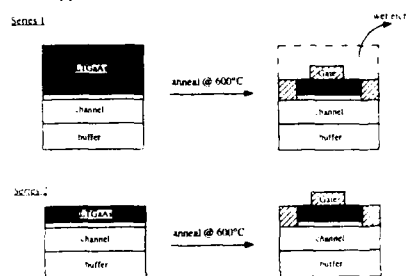


Fig. 4: Schematic showing diodes used to compare effects of the growth surface on the trap distribution during the postgrowth anneal. In one case 5000Å of LTGaAs was grown prior to the anneal and then etched back to the desired thickness. In the other case, the anneal took place following growth of a thinner layer.

As can be seen in figure 5 the V_{th} is considerably smaller in as-grown samples (open circles) when compared to etched-back samples of comparable thickness (solid circles). This suggests significant outdiffusion of excess arsenic during the anneal. From (1) we see that there is roughly a 50% reduction in the average trap density for a 1000Å thick insulator layer when only 1000Å of material is grown prior to the anneal. The flattening of the V_{th} vs thickness curve for the etched back sample for thickness > 3500Å also suggests that the defect diffusion length during the anneal is on the order of 1500Å.

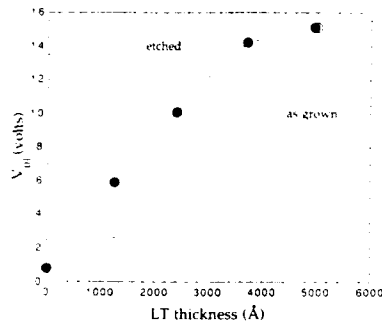


Fig. 5: V_{th} data showing effect of the accessibility of the growth surface during the anneal on the average trap density in a LTGaAs surface layer. Etched back samples (solid circles) displayed a larger V_{th} , and therefore a higher average trap density, than the as-grown samples (open circles). The flattening of the etched sample curve at ~3500Å suggests the defect diffusion length is on the order of 1500Å.

The presence of traps is assumed to improve gate-to-drain breakdown by preventing surface leakage effects, although the exact mechanism by which this occurs is unknown. Nevertheless, it is reasonable to assume that the trap density is an important parameter in obtaining high breakdown. While our results do not differentiate between the structural nature of the traps, they do suggest that precipitate formation can be expected to be inhibited in layers of thickness on the order of the observed defect diffusion length of ~1500Å when compared to precipitate formation in bulk LTGaAs. Work on the correlation between precipitate size and density in the LTGaAs surface layer and MISFET breakdown characteristics is currently under way.

Finally, it is interesting to note the effect of increasing the bias across the device. Under forward bias, all the applied voltage is accommodated across the insulator. Therefore our data enable us to place a lower limit on the breakdown field in LTGaAs (lower limit since the field actually changes sign within the insulator due to the band-bending, as shown in figure 3b). Typically, we found the devices could support ~10V across 2000Å of LTGaAs prior to destructive breakdown, yielding a breakdown field under forward bias of $>5 \times 10^5$ V/cm.

CONCLUSIONS

Current flow through LTGaAs surface layers 1000Å to 5000Å thick is found to be space charge limited. The trap distribution is significantly affected in the vicinity of the growth surface during the annealing of the LTGaAs layer, with a higher trap-filled limited voltage observed in samples grown 5000Å thick and etched back to 2500Å, say, when compared to an as-grown 2500Å thick sample. The data suggest that the diffusion length during the 600°C anneal for excess arsenic related defects is ~1500Å. Breakdown fields $>5 \times 10^5$ V/cm were observed in LTGaAs layers grown at 250°C.

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A GATE BREAKDOWN MECHANISM IN MESFETs AND HEMTs

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ABSTRACT

A model for gate breakdown in MESFETs and HEMTs is proposed. The model is based upon a combination of thermally assisted tunneling and avalanche breakdown. When thermal effects are considered it is demonstrated that the model predicts increasing drain-source breakdown as the gate electrode is biased towards pinch-off, in agreement with experimental data. The model also predicts, for the first time, the gate current versus bias behavior observed in experimental data. The model is consistent with the various reports of breakdown and light emission phenomena reported in the literature.

1. INTRODUCTION

Gate breakdown is important in determining the onset of saturation and the output power capability of microwave field-effect transistors [1-3]. Avalanche breakdown should yield a BVds locus that decreases as the gate is biased towards pinch-off. This is, in fact, the breakdown behavior demonstrated by JFETs. The experimental data for MESFETs and HEMTs, however, generally indicate the opposite behavior [2,3,5,6] (i.e., BVds increases as Vgs is increased towards pinch-off). A model that adequately and accurately explains the measured breakdown performance has not been reported.

The avalanche argument leads to inconsistent predictions in comparison with experimental data. For example, an avalanche mechanism is consistent with observation of light emission under breakdown conditions [2,3,5,6,7]. However, the avalanche model does not adequately explain the detailed behavior of the light emission with bias [3]. The avalanche breakdown model also predicts an

increase in breakdown voltage with temperature, in contrast to the decrease often observed in experimental data. The avalanche model does not predict the observed gate current versus bias voltage behavior under breakdown conditions. The experimental data indicates increasing I_g for increasing V_{gs} at low drain bias, but decreasing I_g for increasing V_{gs} at high drain bias, resulting in a 'twist' in the I_g versus V_{ds} characteristic when plotted for varying V_{gs} .

In this report a new thermal/tunnel/avalanche explanation of gate breakdown is presented and it is demonstrated that the new model adequately explains measured data. The new model allows for both tunneling and avalanche breakdown of the gate electrode. Which mechanism dominates is determined by device structure, bias, channel temperature, and operating conditions. The model also provides an explanation for the success of thin surface insulators formed by low temperature MBE growth in producing significantly increased gate breakdown voltages [8-10].

II. THERMALLY ASSISTED TUNNEL LEAKAGE

Under normal operating conditions breakdown occurs at the drain-side edge of the gate electrode. At this location the electric field is two dimensional with a large horizontal component. Under large drain voltage, but low gate bias (i.e., near I_{dss}), the surface electric field can become sufficiently large that electrons tunnel from the gate metal onto the surface of the semiconductor in the gate-drain region. The tunneling mechanism is enhanced by elevated channel temperature at the gate electrode due to large dc power dissipation at this bias condition. An excess density of electrons can accumulate on the surface of the semiconductor at the gate edge and are free to flow to the drain contact, thereby providing a leakage current and initiating breakdown. The surface resistance is determined by the specific surface conduction mechanism.

As gate bias is increased towards pinch-off the channel current is reduced, resulting in a reduced channel temperature due to less power dissipation. The reduced temperature at the gate electrode produces an increased threshold voltage for the tunnel leakage and the surface current is reduced. The reduced gate leakage allows an increased drain bias to be applied to obtain a constant gate current (e.g., 1 mA/mm), thereby providing an increased drain-source breakdown voltage as gate bias is increased towards pinch-off. As the gate bias nears pinch-off the electric field under the gate electrode becomes more vertically oriented. The electric field can

become sufficient for avalanche breakdown to occur. At this point, the breakdown can consist of a combination of tunneling and avalanche and although the breakdown voltage generally decreases with temperature, increases have also been observed in experimental data.

III. BREAKDOWN MODEL

A model for gate breakdown based upon the above explanation has been formulated. The breakdown mechanism under typical operating conditions is dominated by the tunnel leakage of the gate electrode and this mechanism occurs before avalanche breakdown. The gate leakage model for operation near I_{dss} is based upon the Padovani and Stratton model [11], modified to include effective mass and temperature variations. The leakage current is expressed in the form

$$J_g = J_s \exp (qV'/E') \quad (1)$$

where V' = the voltage across the tunnel barrier at the gate edge

$$E' = E_{00} [E_{00}/kT - \tanh (E_{00}/kT)]^{-1} \quad (2)$$

$$\text{with } E_{00} = 2q\alpha(Nd/2\epsilon)^{1/2} \quad (3)$$

$$\text{and } \alpha = 4\pi(2m^{*'})^{1/2}/h \quad (4)$$

where m^{*} is the adjusted effective mass.

The temperature at the gate electrode is calculated from the power dissipated in the channel under the gate and the thermal resistance of the device. The leakage current flows primarily along the surface of the region between the gate and drain electrodes. In the model the effective mass can be adjusted to give agreement with experimental data.

The gate leakage current versus drain-source voltage characteristic calculated by the model is shown in Fig. 1. The model predicts, for the first time, the 'twist' in the gate current as a function of gate voltage, in agreement with experimental data [2,3].

IV. SURFACE STATE EFFECTS

It is known that negatively charged surface states affect the electric field at the gate edge by providing additional negative charge for termination of the electric field lines emanating from the positive

donor ions in the conducting channel depletion region [12]. Less crowding of the electric field lines occurs at the gate edge and this, in turn, affects the bias voltages required to achieve breakdown conditions. Increased surface electron density produces increased breakdown voltage. A similar phenomenon occurs due to traps located at the conducting channel/substrate or buffer layer interface.

The actual slope of the drain-source breakdown locus with gate bias is significantly affected by the surface treatment of the device. For example, if the surface treatment results in many negatively charged states the threshold for breakdown will be increased. The drain-source breakdown voltage BV_d s can be essentially constant with V_g s. A reduced density of surface electron traps will result in a reduced breakdown voltage, especially for gate bias voltages near I_{dss} . At this bias a reduction by a factor of two in the breakdown voltage over that near pinch-off is often observed in typical GaAs MESFETs.

An ideal surface passivation for power MESFETs and HEMTs would provide a high density of traps near the gate electrode to accommodate injected electrons from the gate and thereby reduce the electric field at the gate edge. The gate electric field relief occurs at the dc bias point and the traps do not have to respond to the RF signal to achieve this benefit. If the traps did respond to the RF field additional benefit would be derived. This passivation layer should also have a low effective electron mobility to reduce the leakage current carried by drifting electrons. The high trap density should accommodate a large trap filled limit voltage which will increase the onset of this leakage current and hence delay breakdown. Lastly, the bulk breakdown voltage of this surface layer should be high to prevent premature surface breakdown. Suitable passivation can be provided by thin surface layers grown by low temperature MBE [8-10].

V. Conclusions

A new model for gate breakdown in MESFETs and HEMTs has been proposed. The model consists of a combination of tunnel leakage and avalanche breakdown of the gate electrode. When the device is biased near I_{dss} the tunnel leakage mechanism dominates. When the device is biased near pinch-off avalanche breakdown can occur. The thermal/tunnel model predicts an increasing drain-source breakdown voltage as gate bias is increased towards pinch-off, in agreement with experimental data. The model also predicts, for the first time, the experimentally observed gate current dependence

upon bias voltage. Finally, the surface leakage model explains the success of thin surface layers of insulating GaAs grown by low temperature MBE in producing significantly improved gate breakdown voltages.

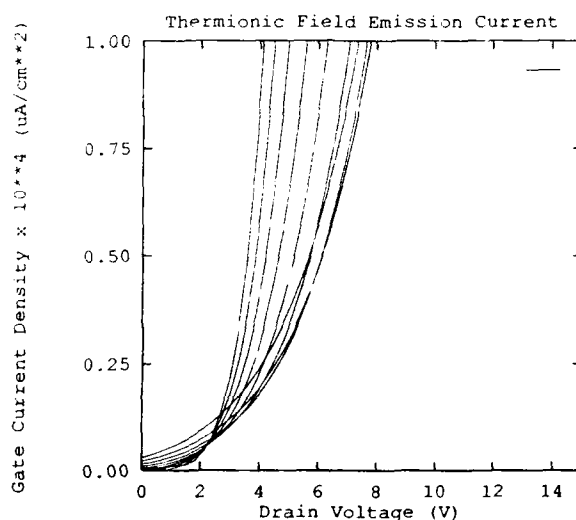


Fig. 1 Gate Current versus Drain-Source Voltage as a Function of Gate Bias Under Breakdown Conditions for a GaAs Power MESFET ($L_g = 0.5 \mu\text{m}$, $W = 1 \text{ mm}$, $\theta = 40 \text{ }^\circ\text{C/W}$)

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ELECTRICAL CHARACTERIZATION OF LOW TEMPERATURE GaAs LAYERS, AND OBSERVATION OF THE EXTREMELY LARGE CARRIER CONCENTRATIONS IN UNDOPED MATERIAL

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ABSTRACT

We present here the results of a study on the effect of substrate temperature, T_s , on the electrical and physical characteristics of low temperature (LT) molecular beam epitaxy GaAs layers. Hall measurements have been performed on the as-grown samples and on samples annealed at 610 °C and 850 °C. Si implantation into these layers has also been investigated.

INTRODUCTION

It has been shown that GaAs buffers grown at low substrate temperatures, commonly known as low temperature (LT) buffers, can be used to eliminate the backgating problem in metal-semiconductor field-effect transistors [1]. LT buffers are of interest because of their electrical, optical, and compositional characteristics [1-4]. In this paper, we present the results of a study on the effect of the growth temperature (substrate temperature, T_s) on the electrical and physical characteristics of LT GaAs layers.

EXPERIMENT

GaAs epilayers were grown on semi-insulating (100) GaAs substrates at a rate of one micron per hour, in a VG V80H molecular beam epitaxy (MBE) system. The substrates were prepared for growth by a standard procedure of degreasing and etching in 7 H₂SO₄ : 1 H₂O : 1 H₂O₂. The As (As₄) to Ga beam equivalent pressure ratio was 18. After the oxide was desorbed from the substrate surface at a temperature of 580 °C, T_s was adjusted to the growth temperature, the sample was stabilized under an As overpressure, and the growth of the GaAs buffer was

started. No post-growth annealing was performed in the MBE chamber.

Sixteen samples were grown at different substrate temperatures (between 100 and 600 °C). Before growing samples 1 ($T_S = 600$ °C) and 2 ($T_S = 500$ °C) the thermocouple used to monitor T_S was calibrated against the congruent sublimation temperature of GaAs. This assures that the quoted T_S values for samples 1 and 2 are quite accurate. However, with decreasing T_S , this calibration becomes increasingly inaccurate. Similarly, pyrometric measurements are inherently inaccurate for low temperatures. Therefore, for samples 3-16, which were grown in a temperature range where no direct calibration is available for the thermocouple, the accuracy of T_S is unknown. However, as described on the next page, the relative values of T_S can be compared using the X-ray calibrations.

Double-crystal X-ray diffraction was performed on all samples. For samples 1-4 ($T_S \geq 460$ °C) and samples 12-16 ($T_S \leq 250$ °C), only one peak was observed in the rocking curves. For samples 5-11 ($260 \leq T_S \leq 450$ °C), two peaks were observed. On this basis, three temperature ranges are defined for T_S : 1) high range, $T_S \geq 460$ °C, 2) intermediate range, $260 \leq T_S \leq 450$ °C, and 3) low range, $T_S \leq 250$ °C. Note that the LT buffers in the literature are grown at a T_S in the intermediate temperature range.

In the high temperature range, the lattice parameter of the epilayer is the same as that of GaAs, therefore the X-ray signals from the GaAs substrate and the epilayer coincide and only one peak is observed. The material grown in the intermediate temperature range was shown to be strongly As-rich, with as much as 2.5 atomic percent excess As in the lattice [1-4]. The extra As incorporated in the lattice results in a perpendicular expansion of the lattice. A typical perpendicular lattice parameter for the epilayer is 5.6595 Å (larger than that of bulk GaAs, 5.6535 Å). Therefore, two rocking curve peaks are observed (one due to the substrate, and one due to the epilayer). Previously, it was reported that for the intermediate range the in-plane lattice parameter is different from that of GaAs [2]. But in this study, the in-plane lattice parameter is equal to that of GaAs. The details of this study will be published elsewhere [5].

In the low range, the epilayer (0.5 micron thick) is amorphous [3] hence the dominant X-ray signal comes from the GaAs substrate and only one peak is seen. For samples 12-16 (the

low range), the epilayers had a gold tint (probably due to the fact that material is amorphous), making them easily distinguishable from the epilayers of the high and intermediate ranges. These showed a color similar to ordinary GaAs. Note that T_S measured in our VG MBE system might be different from others, as explained in the next paragraph.

The transition between the low range and the intermediate range was previously reported as 210 ± 25 °C. This value was based on the growth-dependent critical thickness argument [3]. The difference between this transition temperature and the one reported here (between 250 to 260 °C) is believed to be due to a systematic error in the thermocouple readings for the two MBE machines. In most MBE machines T_S is inferred from a thermocouple reading the temperature of the sample holder. Hence each machine has a different relationship between T_S and the reading taken from the thermocouple. This means that for any MBE system, X-ray measurements must be done on the MBE material in order to define the three ranges of T_S . These measurements can also be used to establish reference points for the thermocouples of different MBE systems.

Due to the high resistivity of the epilayers, Van der Pauw Hall measurements could not be done on any of the 16 as-grown samples. All the samples were annealed at 610 °C for 10 minutes with a GaAs proximity cap. The resistivity of the samples was still too high to permit Hall measurements. The 16 (as-grown) samples were subsequently annealed at 850 °C for 20 minutes with a GaAs proximity cap. For the samples in the high and intermediate ranges, Hall measurements were still not successful, due to the high resistivity of the annealed samples. On the other hand, for the samples in the low range, good ohmic contact could be made to the samples. The resistances between two adjacent contacts on Hall samples (about 0.5 cm apart) varied from 50 to 500 ohms even before alloying the contacts at 430 °C. Hall mobilities varied from 490 to 920 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and net electron concentrations from 8.8×10^{17} to $1.5 \times 10^{18} \text{ cm}^{-3}$. Since the as-grown samples were not doped, these high carrier concentrations can only be due to an intrinsic property of the material grown in the low temperature range.

Next, as-grown samples 1, 2, 3, 8, and 14 ($T_S = 600, 500, 480, 350, \text{ and } 200$ °C, respectively) were ion-implanted with $^{29}\text{Si}^+$ at a fluence of $2 \times 10^{13} \text{ cm}^{-2}$, and an implant energy of 100 keV. Note that samples 1, 2, and 3 are in the high range, sample 8 is in the intermediate range, and sample 14 is in the low range. The implanted samples were capped with silicon

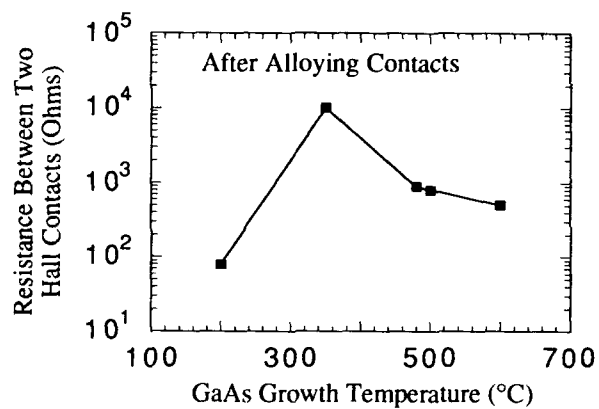


FIG. 1. Resistance between two adjacent indium contacts on Hall sample versus growth temperature, for the samples implanted with $^{29}\text{Si}^+$ at a fluence of $2 \times 10^{13} \text{ cm}^{-2}$ and annealed in furnace at 850°C for 20 minutes.

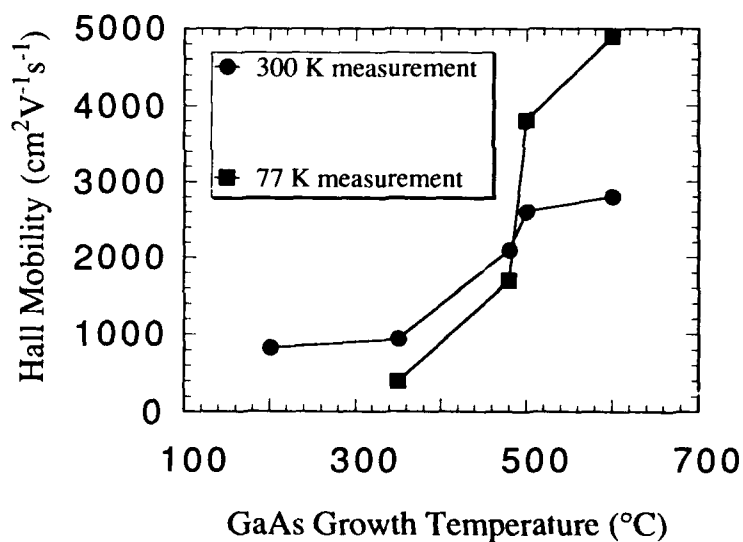


FIG. 2. Hall mobility versus growth temperature, for samples of figure 1.

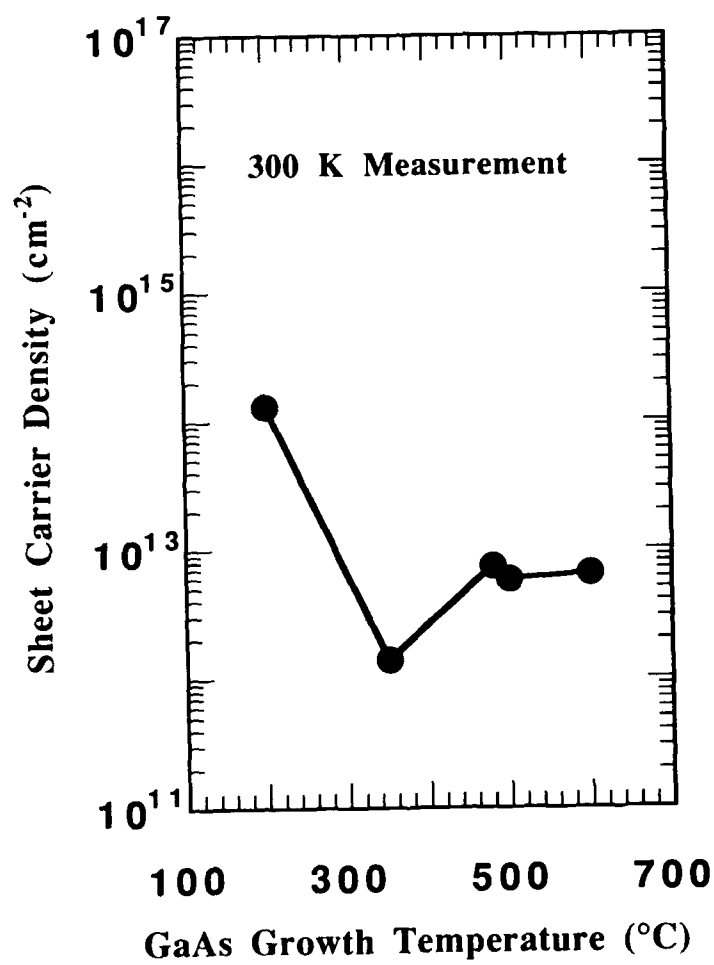


FIG. 3. Net sheet electron density versus growth temperature, for the samples of figure 1.

nitride, and annealed in the furnace at 850 °C for 20 minutes. After removing the caps, Hall measurements were performed. Figures 1, 2, and 3 show resistance between two adjacent Hall contacts, Hall mobility, and net sheet electron density, respectively. Both the 300K and 77K mobilities monotonically increase with T_S . This may seem intuitive, since as T_S decreases material quality degrades and defect density increases, hence mobility decreases. However, figure 3 is not as intuitive. In figure 3, the sheet carrier density for the low range sample (sample 14, grown at 200 °C) is surprisingly large ($1.3 \times 10^{14} \text{ cm}^{-2}$). This is larger than the fluence of the Si implantation ($2 \times 10^{13} \text{ cm}^{-2}$). Again, this large sheet carrier density can only be due to an intrinsic property of this material. It has nothing to do with the activation of implanted Si. The carriers are probably originated from some defects in the amorphous GaAs, activated by the high temperature annealing.

Since the resistance between two Hall contacts is inversely proportional to the product of sheet carrier density and mobility, figure 1 is reflected in figures 3 and 2. The small resistance between two contacts for the sample grown at a T_S of 200 °C is due to the large sheet carrier density in this film.

From an electrical stand point, the most striking difference between the low range and the intermediate range is the fact that after annealing at 850 °C the undoped layers grown below or at 250 °C have a low resistivity (net electron concentrations as high as $1.5 \times 10^{18} \text{ cm}^{-3}$ and mobilities as high as $920 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$), while after anneal the undoped layers grown in the intermediate range have extremely high resistivity (about $8 \times 10^5 \text{ ohm.cm}$) [1-4].

We would like to thank Mr. Goldenberg and Mr. Mittereder.

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ULTRAFAST PROPERTIES AND APPLICATIONS OF GaAs AND InP BASED MATERIALS GROWN BY MBE AT LOW TEMPERATURES

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ABSTRACT

The ultrafast carrier dynamics in GaAs, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ on InP, and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ on InP, grown by molecular-beam-epitaxy (MBE) at low substrate temperatures, are investigated. A reduction in the carrier lifetime is observed with decreasing growth temperatures. The shortest carrier lifetimes of typically a picosecond (ps) are obtained at the lowest growth temperature range of 150 - 200 °C. Femtosecond optical absorption and reflectance measurements have been used to verify the sub-picosecond carrier lifetimes. Photoconductive switching measurements on these materials, measured using the technique of electro-optic sampling have further confirmed the sub-picosecond carrier lifetimes, and have also resulted in the generation of subpicosecond electrical signals. These short electrical pulses have been used for a variety of ultrafast optoelectronic applications.

LOW TEMPERATURE MBE GROWTH AND MATERIAL PROPERTIES RELATING TO CARRIER DYNAMICS

Introduction

For conventional, high optical and electrical quality epitaxial growth by MBE, the substrate is heated to ~600°C and ~500°C for GaAs and InP substrates, respectively. The substrate temperature (T_s), the group V/III flux ratio and the growth rate are important parameters in determining the growth mechanism and the quality of the epitaxial layers. Smith et al. [1] were the first to demonstrate the interesting properties of GaAs grown by MBE at T_s ~200°C at the usual growth rates of ~1µm/hr, where it was used as a high resistivity buffer layer, completely eliminating the side-gating and back-gating effects in GaAs MESFETs. Since then a number of detailed characterization of the material properties of the low-temperature (LT) MBE grown layers has been undertaken [2]-[6]. Some of these are summarized below, which are pertinent to the understanding of the ultrafast carrier dynamics.

Low-temperature MBE of GaAs

For the LT-MBE grown GaAs layers, Ga and As_4 beam fluxes were used at a V/III beam equivalent pressure ratio of 10. The growth rate is 1.0 µm/hr on (001)-oriented semi-insulating GaAs substrates. First an undoped buffer layer of GaAs is grown at a temperature of 600°C to smoothen the growth front. Next the substrate temperature is lowered down to the desired value, and typically 1-2 µm thick LT-GaAs layer is grown. A range of growth temperatures was investigated : 400, 350, 300, 260, 200 and 190°C. Some of the layers were then annealed inside the growth chamber under the As-overpressure by raising the substrate temperature to about 600°C for a period of 3-10 min. All the layers studied here (1-2 µm thick) were of high

crystalline quality, as also verified by their reflection-high-energy-electron-diffraction (RHEED) pattern during growth.

These LT-GaAs layers are grown under highly As-rich conditions. Due to the low T_s , the residence time of As-adatoms on the growing surface increases. Hence excess As in the form of interstitials (As)_i, antisite defects (As)_{Ga}, As-microclusters, or gallium vacancies (V)_{Ga} are expected [2]. Auger Electron Spectroscopy (AES) has shown about 1% excess As (10^{20} cm^{-3}) in the 200°C as-grown and annealed LT-GaAs film [3]. Electron Paramagnetic Resonance (EPR) measurements have indicated [4] that in the as-grown material about 5% of this excess As is ionized, whereas in the annealed material this drops down below the detection limit of 10^{18} cm^{-3} . From infrared absorption measurements this value is estimated to be in the range of 10^{17} - 10^{18} cm^{-3} for the annealed 200°C LT-GaAs material [2]. These observations lead to a defect-band-model of the 200°C LT-MBE grown GaAs for the as-grown and annealed material. This is discussed in detail in reference [2]. Fig.1 gives a picture of the density of states and the relevant parameters for the annealed 200°C LT-GaAs material.

After another layer is grown on top at normal temperatures (600°C), or the layer is annealed at a high temperature for a few minutes, As-precipitates have been observed by TEM [5]. The average diameter of the precipitates is 60 Å, and their density is of the order of 10^{17} to 10^{18} cm^{-3} . An important conclusion can be drawn regarding the carrier (electron and hole) dynamics in this material from this As-precipitate model as shown in Fig.1. We approximate the capture cross section of the carriers by the projection of the occupied volume of the As-precipitate on a plane perpendicular to the velocity of an incoming carrier, i.e.

$$\sigma = \pi (d^2 / 4) = 2.83 \times 10^{-13} \text{ cm}^2 \text{ for } d = 60 \text{ Å} \quad (1)$$

Next we consider the defect-band model for the carrier recombination mechanism from the extended band states into these midgap states, namely the Shockley-Read-Hall (SRH) recombination statistics [7]. The minority carrier lifetime in this model, for the low injection regime, is given by Eqn.(2).

$$\tau_c = 1 / N_t \sigma v_{th} \quad (2)$$

where τ_c = carrier lifetime, N_t = density of traps = $5 \times 10^{17} \text{ cm}^{-3}$ (average value in the annealed 200°C LT-GaAs material), $\sigma = 2.83 \times 10^{-13} \text{ cm}^2$ from Eqn.(1), v_{th} = thermal velocity = $2.5 \times 10^7 \text{ cm/s}$ (at room temperature). Substituting one finds $\tau_c < 1 \text{ ps}$. Either both types of carriers are trapped at the same midgap defect band, and thus recombine, i.e. this acts as a recombination center, or the midgap donor and acceptor levels capture carriers, which then recombine.

Low-temperature of InP based materials

From the above discussion of the properties of the LT-GaAs layer, it is seen that its unique properties are related to a significant excess As-rich condition, while still preserving its crystallinity. Therefore similar behavior might be expected of the low-temperature MBE growth of other As-containing III-V materials e.g. lattice-matched/mis-matched InAlAs and InGaAs on InP. In order to study this, a number of layers of lattice-matched $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ were grown by MBE at low temperatures on semi-insulating InP substrates.

A series of 1- μm -thick $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers were grown on Fe-doped semi-insulating (100) InP substrates by MBE at successively reduced temperatures of 480, 400, 300, 200, and 150°C, at a growth rate of 0.6 $\mu\text{m/hr}$ [7]. The V/III flux ratio was maintained at 45. Growth was done on As-stabilised (2x4) reconstructed surface as observed in the in-situ RHEED pattern before and after growth. A sample grown at 150°C was annealed in-situ under an arsenic overpressure by raising the substrate to 500°C for 10 min. after the growth was

completed. Nominally undoped layers of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ grown by MBE at temperatures of less than 500°C are insulating [8]. Therefore low temperature MBE grown $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers when used as buffer layers for FET's, have shown remarkable improvements in the performance of these devices [9].

A systematic study of the structural quality and arsenic content of the as-grown $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers described above has recently been reported [10]. It is observed that $1\text{ }\mu\text{m}$ thick layers can be grown on InP with a high crystalline quality for growth temperatures down to 200°C . The amount of excess-As incorporated generally tends to increase as the growth temperature is lowered. At lower growth temperatures of 150°C , the material is not monocrystalline and a high density of pyramidal defects are formed, mostly consisting of dislocations and hexagonal-As. Thus the behavior is qualitatively similar to the case of LT-GaAs, where the excess-As is also incorporated and leads to As-precipitate formation under certain conditions as described in previous sections. Therefore short carrier lifetimes are also expected in LT- $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$.

In contrast, lattice-matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ grown around 500°C is n-type and is virtually trap free. For our preliminary study of low temperature MBE in this material system, a series of $1\text{-}\mu\text{m}$ -thick undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers were grown at successively reduced growth temperatures of 500 , 300 , 200 , and 165°C , on a $0.3\text{ }\mu\text{m}$ undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ buffer grown at 500°C on a (001) oriented InP substrate. The samples were grown at a rate of $\sim 1\text{ }\mu\text{m/hr}$ with a group V/III beam equivalent pressure ratio of 10. All the samples appear to be crystalline as observed by RHEED.

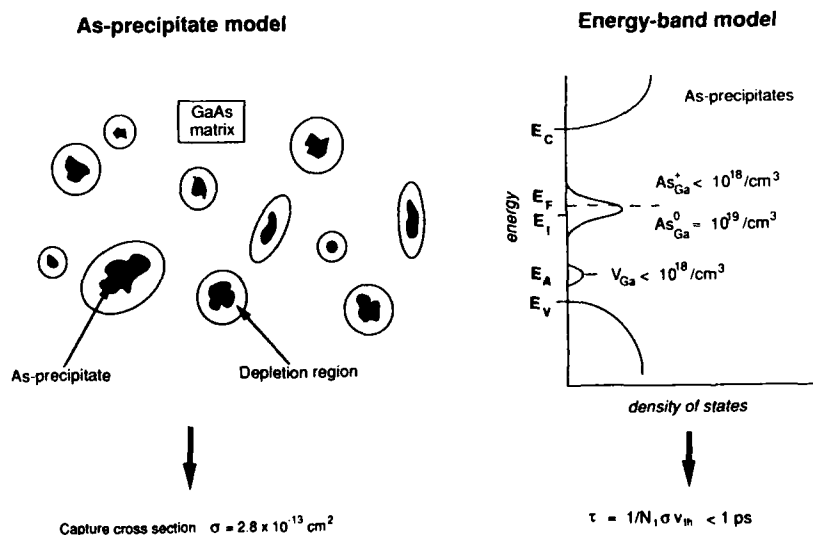


Fig. 1 Energy band model and As-precipitate model for LT-GaAs grown at 200°C .

FEMTOSECOND OPTICAL REFLECTANCE / ABSORPTION MEASUREMENTS

To measure the carrier lifetime in LT-MBE grown materials, the technique of time-resolved photoluminescence would appear to be the most direct approach. However due to the high density of deep-level defects as mentioned above, and consequently the recombination being dominated by non-radiative processes, this approach is not possible. Carrier injection, either electrically or optically, causes a number of induced absorption changes through the processes of bandfilling, band-gap renormalization, and free-carrier absorption [11]. The time-evolution of this induced absorption and reflection change is thus a measure of the carrier lifetime.

Experiment

The basic experimental schematic is the familiar pump-probe arrangement. An ultrashort pulse (typically ~ 100 femtoseconds) laser source is divided into two beams. The excitation beam is focussed to a ~ 20 - $30\ \mu\text{m}$ and impinges on the semiconductor sample, thus generating carriers. The probe beam, passes through a variable optical delay line is focussed to a slightly smaller spot (~ 10 - $20\ \mu\text{m}$), overlapping the pump spot. The probe beam power is attenuated by a factor of 10, as compared to that of the pump beam. To avoid unwanted interference effects or coherent artifacts, the probe beam polarization is made orthogonal to that of the pump beam or is made circularly polarized.

For most of our measurements, a visible colliding pulse mode-locked (CPM) ring dye laser is used. This laser typically produces 120 fs full-width-half-maximum (FWHM) pulses, centered around a wavelength $\lambda = 620\ \text{nm}$, with a repetition rate of 100 MHz. The time resolution of this pump-probe measurement is given by the cross-correlation of the pump and

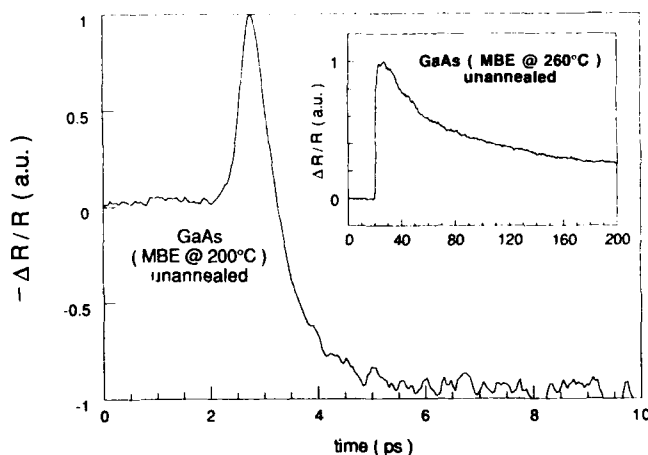


Fig. 2 Transient optical reflectivity using CPM laser for unannealed 200°C MBE grown LT-GaAs. Inset shows the same measurement for unannealed 260°C MBE grown LT-GaAs.

probe laser pulses and is ~ 250 fs. For some measurements, as will be discussed in the next section, a self-mode-locked femtosecond Ti-sapphire laser is used.

Results and discussion

Figure 2 shows a typical data for LT-GaAs grown at 260°C (inset) and 200°C . Fig. 3 plots the carrier lifetime as a function of the growth temperature for the unannealed samples, as obtained from the initial $1/e$ decay of the transient reflectivity signature. Thus it is observed that the carrier lifetime decreases with a decrease in the growth temperature, with a sub-picosecond value for the lowest growth temperature range [12].

On a closer look a number of features need to be understood about the data in Fig. 2. First let us consider the data for LT-GaAs grown at temperatures of 260, 300, 350 and 400°C , all of which show similar decay curves, with the decay times as given in Fig. 3. The initial photoinjected carrier density is estimated to be $\sim 1.0 \times 10^{18} \text{ cm}^{-3}$. The Δn resulting from this carrier induced bandfilling, bandgap renormalization and free carrier absorption is estimated to be 2.87×10^{-3} , -1.42×10^{-3} and -8.7×10^{-4} , thus giving a total initial Δn ($t=0$) = 5.8×10^{-4} . Experimentally the Δn signal is positive and the amplitudes fall between 4.0 - 6.0×10^{-4} , in close agreement with the value given above.

For the samples grown at 200 and 190°C , the initial decay time is measured to be less than 0.4 ps. Two additional features are observed in the reflectivity data of the unannealed 190 and 200°C LT-GaAs layers. First, the initial change in reflectivity is negative for times less than 1 ps after the pump laser pulse is incident on the sample surface. The second interesting feature is the crossing of the zero axis and the subsequent slow recovery (~ 10 -15 ps) of the signal. At present we do not have a clear understanding of why the initial $\Delta R/R$ transient is negative in the as-grown samples, but we speculate that it could be due to a large density of near band-edge states that give rise to a larger and smeared out band-edge absorption. This would greatly decrease the effect of bandfilling and bandgap renormalization on Δn , resulting in the dominant contribution to Δn being from free carrier absorption, which is negative. We believe that the slowly recovering component of the signal is not indicative of the carrier lifetime, as inferred from the transient reflectivity measurements on the annealed samples to be discussed in the next paragraph. It is possible that this slow transient in $\Delta R/R$ arises from re-emission of carriers from near band-edge states into the conduction and/or valence bands and the subsequent fast recombination of the free carriers.

The transient reflectance signal observed for LT-GaAs grown at 260°C or above show no significant difference between the as-grown and the annealed samples. However, annealed samples grown at 190 and 200°C displayed essentially the same subpicosecond decay observed for the unannealed samples, except that $\Delta R/R$ is positive and there is a negligible slow component as shown in the inset of Fig. 4. These results lead us to conclude that the carrier lifetime in LT-GaAs is primarily determined by the growth temperature and not by the annealing, and that the As-precipitates present in the annealed material are not necessary to achieve the fast recombination times.

It should be remembered that the photoexcitation of carriers for the above mentioned experiments using a CPM laser at $\lambda = 620 \text{ nm}$ (2.0 eV) occurs far above the GaAs band edge ($E_g = 1.42 \text{ eV}$). Hence the initial injected carriers have almost 0.6 eV of excess energy. Therefore, intraband carrier relaxation by optical phonon emission and inter-valley scattering can play a significant role in determining the reflectance change especially on the sub-picosecond time scale. Therefore to estimate the actual carrier lifetime in the LT-GaAs material on the sub-picosecond time scale it is preferable to photoinject carriers at an energy slightly above the band-gap so that the scattering to the satellite valleys is completely eliminated and the

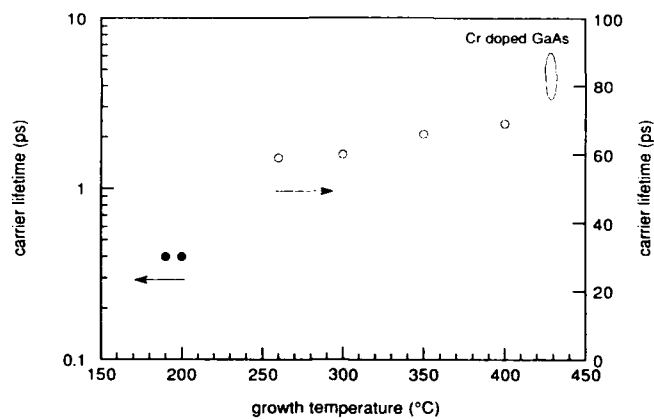


Fig. 3 Carrier lifetime v/s growth temperature for low-temperature MBE grown GaAs, measured by transient reflectance using CPM laser.

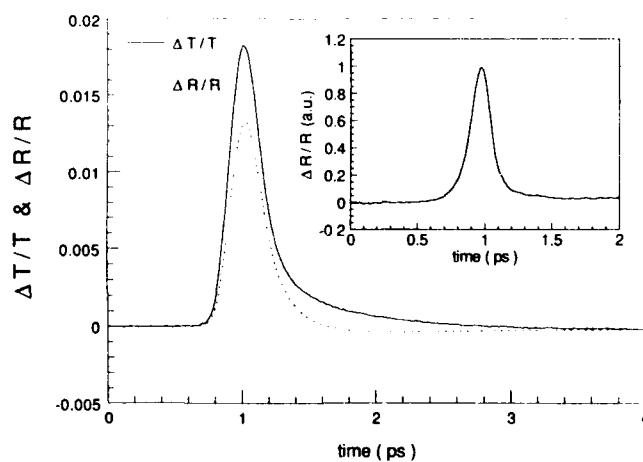


Fig. 4 Transient reflection and transmission for annealed 200°C LT-GaAs using Ti-sapphire laser at $\lambda=835$ nm. Inset shows the same measurement using CPM laser at $\lambda=620$ nm.

intraband relaxation is minimized to one or two LO-phonon emission. For this a self-mode-locked Ti-sapphire laser. This laser generates 100 fs FWHM pulses, and the wavelength is tuned to $\lambda = 835$ nm, i.e. ~ 60 meV above the GaAs band edge. Hence intervalley scattering is completely eliminated, and intraband relaxation by LO-phonon emission is minimized. Hence the primary process for the change in Δn on a subpicosecond time scales is due only to the trapping of carriers. The results of such a measurement are shown in Fig. 4. For this measurement an annealed LT-GaAs epitaxial film grown at 200°C was used. Also by selectively etching the substrate, a back-hole is opened so that simultaneous reflection and transmission measurements can be made. The fractional changes are larger, about 1-2%, as compared to the measurements done using a CPM laser at $\lambda = 620$ nm. The carrier induced refractive index change increases rapidly near the band edge, in fact a resonance occurs. Hence larger signals are expected for measurements closer to the band edge. From the measurement one can estimate the carrier lifetime of the 200°C LT-GaAs material to be about 0.3 ps.

It was pointed out that the unique properties of LT-GaAs is attributed to the significant As-rich conditions in the material and therefore similar properties can be expected in other As-containing III-V compounds. Fig. 5 shows the time-resolved reflectance measurement of these LT- $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ samples, using a CPM laser [7]. A gradual reduction in the initial fall time from ~ 12 ps to ~ 4 ps is observed as the growth temperature is lowered from 480°C to 200°C . For the sample grown at 150°C , a drastic reduction in the fall time to ~ 0.4 ps is observed. Note also that the reflectivity signal from this sample is inverted and crosses the zero axis with a slowly recovering component. This behaviour is exactly similar to the one observed for LT-GaAs layers as mentioned above and similar arguments can be made for the LT-InAlAs layers. Fig. 6 plots the carrier lifetime as a function of the growth temperature for the unannealed LT- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers grown on InP substrate. The carrier lifetime is also observed to decrease with decreasing growth temperatures in this material system and reaches a value of about 2.5 ps for the lowest growth temperature investigated.

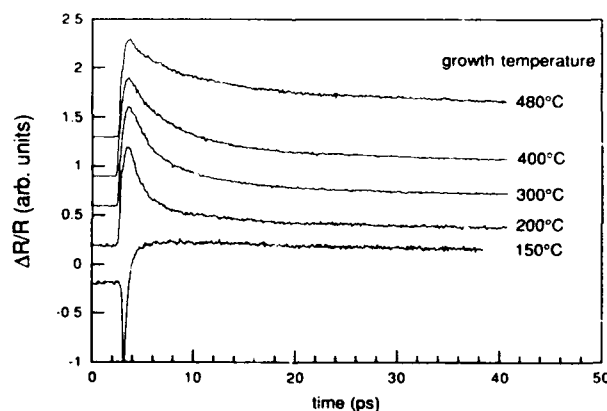


Fig. 5 Time-resolved reflectance of unannealed low-temperature MBE grown $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ at $\lambda = 620$ nm.

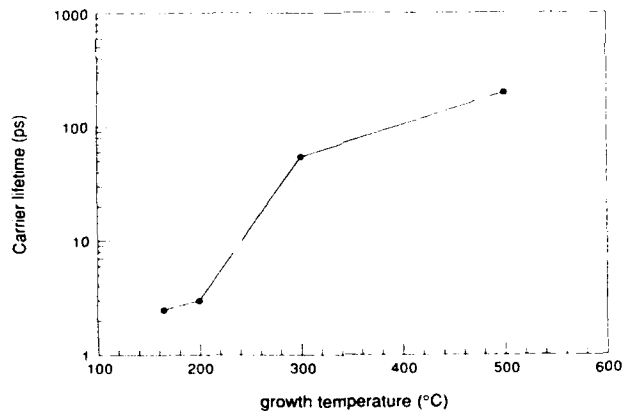


Fig. 6 Carrier lifetime v/s growth temperature for low-temperature MBE grown $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epilayers.

PHOTOCONDUCTIVE SWITCHING MEASUREMENTS

Experiment

For measuring the high speed response of passive or active devices, directly in the time-domain, electro-optic sampling [13] is emerging as the most useful technique. This technique exploits the fast Pockels effect, in which an electric field applied to a nonlinear crystal, changes the birefringent properties of the crystal, and therefore the polarization of the light passing through it. Hence if the crystal is placed between crossed polarizers, the transmitted light intensity changes as a function of the applied field. Many different embodiments of the electro-optic sampling can be implemented. The one used here is the external 'finger-probe' scheme [14]. A CPM dye laser is used as the short pulse source. The temporal response of this technique is limited to about 300 fs.

Results and discussion

From the above discussion it appears that low-temperature MBE grown GaAs, especially those grown around 200°C, has the desired properties of a fast photoconductor. Fig. 7 shows the measured photoconductive switch response of the LT-GaAs film grown at 200°C and annealed at 600°C for 10 min. inside the growth chamber under an As-overpressure, after the completion of the growth. The electrode geometry is a coplanar waveguide with a wave impedance of 50Ω. A 10-μm-gap in the center electrode serves as the photoconductive generating gap. An electrical signal is launched by shorting the gap in the 10 V dc-biased center

line, using a beam from the CPM laser. The signal is then detected using the finger-probe electro-optic sampling as described earlier. The detection is done about 150 μm from the generating gap to keep the distortion of the propagating pulse to a minimum. The pulse has a nearly symmetric shape and a FWHM of 0.6 ps. Note that this is the directly measured pulsewidth, that is without deconvoluting any effects. This represents the shortest photoconductively generated electrical pulse in a III-V material. From the $1/e$ decay time of the electrical pulse in Fig. 7, the carrier lifetime in the 200°C annealed is estimated to be less than 0.4 ps. Note that this value is consistent with the time-resolved reflection/absorption measurements. This is expected since both are primarily determined by the photoexcited carrier lifetime. Writing the integrated photocurrent as

$$I_s = \frac{V_s}{Z_0} = \eta(1-R) \frac{e}{\hbar\omega} \mu \tau \frac{V_b}{l^2} P \quad (3)$$

where Z_0 = characteristic impedance, η = quantum efficiency (~ 1.0), R = reflectivity, μ = mobility, τ = carrier lifetime, V_b = applied bias, l = gap length, and P = average optical power, and substituting the relevant experimental parameters, one computes a value of $\mu = 120 - 150 \text{ cm}^2/\text{V}\cdot\text{s}$ for the LT-GaAs material. This is compared to a value of about $30 \text{ cm}^2/\text{V}\cdot\text{s}$ typically obtained for implanted SOS material, so far the most popular photoconductive material for generating short electrical pulses. Hence a better efficiency is obtained in generating short pulses.

We have seen earlier that subpicosecond carrier lifetimes have been observed in other low-temperature MBE grown III-V materials. Therefore it is important to know their photoconductive switching behavior. Fig. 8 shows the photoconductive switch response measured by external electro-optic sampling for the LT- $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ sample grown at 150°C. Three cases are shown: unannealed, externally annealed and in-situ annealed. It is seen that in the former two cases, the subpicosecond $1/e$ fall time of ~ 0.5 ps is maintained which matches very well with the fall time of ~ 0.4 ps as obtained from the time-resolved reflectivity data. However with in-situ anneal, the switching response slows down to 1.2 ps as is also indicated by the decay time from the transient reflectance data. The in-situ annealed material also exhibits a fairly long decay component (~ 10 ps) in the photoconductive response. The responsivity is seen to improve marginally with external anneal and moderately with in-situ anneal. The best responsivity translates into an approximate value of $\mu \sim 5 \text{ cm}^2/\text{V}\cdot\text{s}$, for the photoconductive switch response. Further study is needed to optimise the performance of this material when used as a photoconductive switch. Nevertheless, the above switching measurements confirm the sub-picosecond carrier lifetimes in this material.

The more interesting material for photoconductive applications is $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. This material has a lower bandgap, around the commercially important wavelength region of 1.5 μm . Hence LT- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ can potentially offer advantages for fast detectors, if similar high resistivity photoconductive switches, with short carrier lifetimes and high responsivity can be demonstrated. Unfortunately the low resistivity of the low-temperature MBE grown lattice-matched InGaAs on InP substrate, has so far precluded their use in photoconductive switching. Further work is needed to increase the resistivity of this material, so as to be useful as a photoconductor switch.

APPLICATIONS

The LT-MBE grown layers have found numerous applications. As mentioned earlier, the high-resistivity nature of these layers have enabled their use as buffer layers for FET's, eliminating the back-gating and side-gating effects.

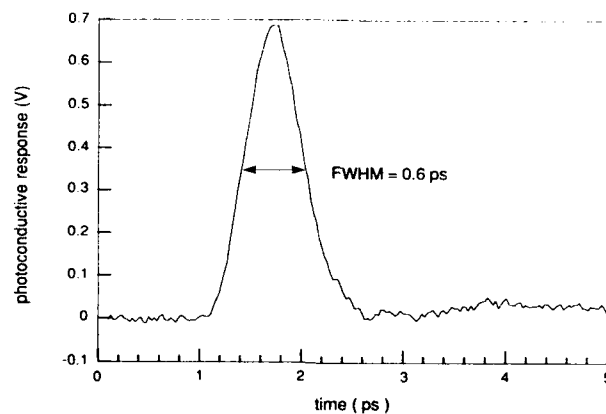


Fig. 7 Photoconductive switch response of annealed 200°C MBE grown LT-GaAs as measured by electro-optic sampling. The applied bias is 10 V across a 10 μm gap.

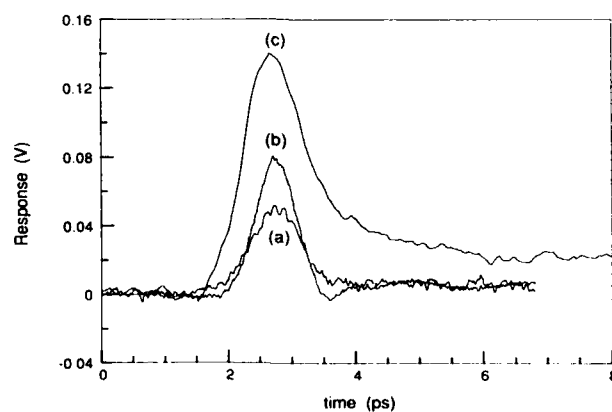


Fig. 8 Photoconductive switch response of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ grown by MBE at 150°C for (a) unannealed, (b) externally annealed, and (c) in-situ annealed samples.

The above mentioned photoconductive switching measurements have enabled the generation of sub-picosecond pulses, i.e. with terahertz bandwidths, with good conversion efficiencies. Also a photoconductive gap in the LT-MBE layers can be used as sampling gates with sub-picosecond resolution. Since the carrier lifetime is very short, most of the carriers recombine before they reach the other electrode in the photoconductive structure. Therefore reducing the gap length would enable the collection of more carriers and hence improve the responsivity. 375 GHz LT-GaAs photodetectors with a responsivity as high as 0.1A/W have been demonstrated [15].

The terahertz bandwidth pulses can also be used to study the microwave performance of passive or active devices. The pulse propagation on coplanar transmission line interconnects have been studied, where the role of dispersion and loss mechanisms have been detailed [16]. Due to the high breakdown strength of these LT-MBE layers, they have also been used to switch high voltage pulses on a picosecond time scale [17]. Thus these LT-MBE grown materials are useful for a number of ultrafast optoelectronic applications.

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A HIGH PERFORMANCE OPTICALLY GATED HETEROSTRUCTURE THYRISTOR PASSIVATED WITH LT-GaAs

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ABSTRACT

A high performance, $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ based, optically gated thyristor with a bulk semi-insulating(SI) GaAs $650\ \mu\text{m}$ in thickness as the voltage blocking layer has been fabricated and characterized for high power pulsed switching applications. Low temperature(LT) GaAs was used to passivate the device surface and was found to greatly improve the switch hold-off voltage. The switched current as a function of bias up to 2,200 V (34 kV/cm) has been tested and the maximum switched current was 240 A with a di/dt equal to 2.02×10^{10} A/s. The forward dynamic current-voltage characteristics have been measured and the dissipated energy per switching determined. It was found that very sensitive triggering of the switch is possible, even with a light emitting diode operating in the sub-mW range, when the thyristor is reverse biased. The sensitive triggering is a result of the carrier tunneling through the reverse biased pn junctions.

INTRODUCTION

Semiconductor heterojunction optothyristors based on $\text{AlGaAs}/\text{GaAs}$ are potentially very suitable for high power and high pulse repetition frequency(PRF) switching applications since the wider band gap AlGaAs can provide an optical window for sensitive optical gating and the bipolar junction can provide high di/dt rating. When compared to the widely used high power device material, Si, direct band gap GaAs allows efficient absorption and generation of photons and should switch faster due to its higher carrier saturation velocity. Also due to its larger band gap, GaAs can tolerate higher temperature and higher radiation energy. Researchers in Ioffe Institute have reported epitaxially grown $\text{AlGaAs}/\text{GaAs}$ optothyristors with hold-off voltage up to 1,000 volts, and di/dt values of 5×10^{10} A/s with peak current close to 10 A have also been reported [1-6]. Interesting results on homojunction GaAs thyristors with SI-GaAs as the voltage blocking layer have also become available recently with a DC blocking voltage of more than 800 V and a di/dt equal to 1.5×10^{10} A/s for close to 300A peak current [7].

In this paper, we report a study of an MBE grown $\text{AlGaAs}/\text{GaAs}$ based optothyristor for high power pulsed switching applications with a $650\ \mu\text{m}$ SI-GaAs as the voltage blocking layer. AlGaAs is used as an optical window for sensitive optical gating and heavily doped P^+ and N^+ epilayers are used for forming good ohmic contacts. Both sides of the device surface are passivated by MBE GaAs grown at very low temperature[8,9] which is found to greatly increase the hold-off voltage.

DEVICE FABRICATION AND MEASUREMENT CIRCUIT

An undoped LEC GaAs with both sides polished was used as the voltage blocking layer. The thickness is $650\mu\text{m}$ and the resistivity is larger than 1×10^6 ohms-cm. A $3 \times 10^{17} \text{ cm}^{-3}$ Be-doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ film of $1.2\mu\text{m}$ in thickness was grown by MBE on one side of the SI-GaAs, followed by a $0.9\mu\text{m}$ $1 \times 10^{18} \text{ cm}^{-3}$ Si-doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer. An undoped $0.2\mu\text{m}$ low temperature(LT) GaAs layer was then grown at 200°C for surface passivation. On the other polished side of the SI-GaAs a $1.2\mu\text{m}$ $1 \times 10^{17} \text{ cm}^{-3}$ Si-doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ film was then grown, followed by a $0.9\mu\text{m}$ $5 \times 10^{18} \text{ cm}^{-3}$ Be-doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer. A $0.2\mu\text{m}$ thick undoped LT-GaAs layer was also grown at 200°C for surface passivation [8,9]. The sample was then annealed in the MBE growth chamber at 580°C for 20 minutes to stabilize the LT-GaAs.

Standard photolithography was used to fabricate recessed circular ohmic contacts of diameter 0.5 cm with an optical aperture 0.1 cm in diameter. Two contacts were made on the top and bottom surfaces. AuGe and AuZn were used for the ohmic contacts on the N^+ side and the P^+ side of the device, respectively. Mesa etching was finally used to define a junction area of 0.79 cm^2 on both sides. The final device, device No.1, is shown in Fig.1. Low inductance connections were used to connect the device to the measurement circuit as shown in Fig.2 where a special low inductance current viewing resistor(CVR) and capacitor have been used to minimize the circuit inductance. The purpose is to minimize the induction oscillation, $L di/dt$, due to the fast current rate of rise, where L is the inductance. A GaAs light emitting diode(LED) operating at $0.88\mu\text{m}$ and a laser diode at $0.904\mu\text{m}$ were used as the light sources. The laser energy is $0.3\mu\text{J}$ with pulse width equal to 30 ns and is optical fiber coupled to the device. A TEK 7104 1GHz fast scope is connected to a TEK DCS digitizing camera system and controlled by a computer for data acquisition. For comparison purpose the same device fabrication procedure was also used to fabricate bulk photoconductive switches using the $650\mu\text{m}$ thick SI-GaAs without any epilayers. AuGe was used for metallization on both sides of the SI-GaAs. This bulk device is named No.2 in the following discussion. Pulsed operation of the devices has been studied and the optothyristor hold-off voltage has been tested up to $2,200\text{ V}$ and $-2,200\text{ V}$ under forward and reverse biases which represents a field intensity around 34 kV/cm . Instead of using a large laser system of more than 30 MW power, We have used an LED of a few mW and a laser diode of 25 W peak power for this study.

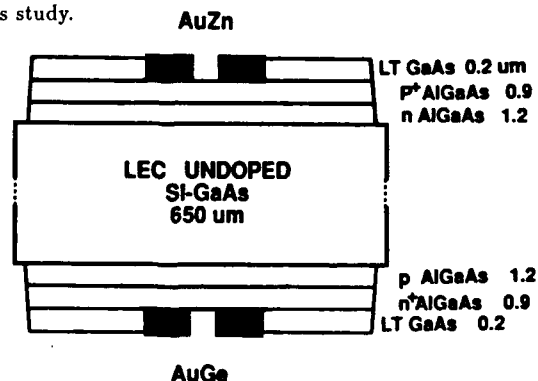


Fig.1 MBE grown optothyristor structure.

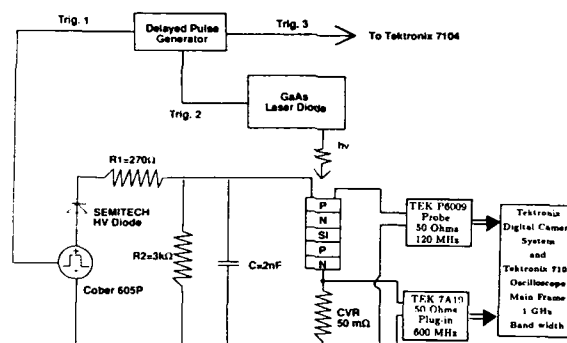


Fig.2 Circuit diagram for laser activated optothyristor testing

EXPERIMENTAL RESULTS AND DISCUSSION

Shown in Fig.3(a) is a 500V/400 μ s bias pulse across device No.2(curve A) and the switching voltage across the device with a constant background illumination by a 10.5mW GaAs LED(curve B). The LED was positioned at the center of the aperture at the N⁺P side of the device and the illuminated area had a diameter of about 0.5 cm. It is seen that the turn-on is not smooth as shown in Fig.3(a), curve B. It is believed that the non-smooth turn-on is a result of the local high field near the metal contact where carriers are photo-generated, of impact ionization of trapped carriers near the metal contact, and of the carrier injection directly from metal contact[10]. This point becomes much clearer when compared to the results of the LT-GaAs passivated device No. 1 with good ohmic contacts and optical windows under exactly the same experimental conditions. Fig.3(b) shows a negative -500V/400 μ s bias pulse across the device(curve A) and the switching voltage across the device with LED illumination power at 0.01, 0.02, 0.04, 0.07, 0.2, 1.04, 1.28, 1.53, 1.77, and 2.00mW (curves B through K). Very smooth turn on is also observed under higher bias and Fig.3(c) shows a negative -1,300V/3.5 μ s bias pulse across the device(curve A) and the switching voltage across the device with LED illumination power at 1.9, 2.5, 3.2, 4.4, 5.7, 7.0, 8.2, 9.3, and 10.5 mW. It is seen that the turn-on of the device is very smooth and the optical gating efficiency is much higher as reflected in the much shorter delay time for turn-on. In particular, comparing curve B in Fig.3(a) and curve C in Fig.3(b) it is seen that for the same delay time the required LED power is reduced from 10.5 mW to 0.02 mW, a reduction of 525 times. This is clearly due to the use of the wider band gap AlGaAs which allows photons be absorbed deep into the device more effectively and the photo-generated carriers be further separated away from the metallization and the semiconductor surface where large surface states exist. In short, bulk turn-on is observed if photons can be effectively pumped deep into the device and be far away from surface states. Although the device reliability has not been studied directly, by comparing curve B in Fig.3(a) with the smooth switching curves in Fig.3(b) and (c) it is expected that the device lifetime can be greatly improved through the improvement of ohmic contacts as well as the removal of the photo-generated carriers from near the metallization and semiconductor surface. Another interesting observation is that the device does not turn on if the device bias pulse changes polarity while other conditions are kept the same. This is due to the large tunneling current of the highly reverse biased pn junctions.

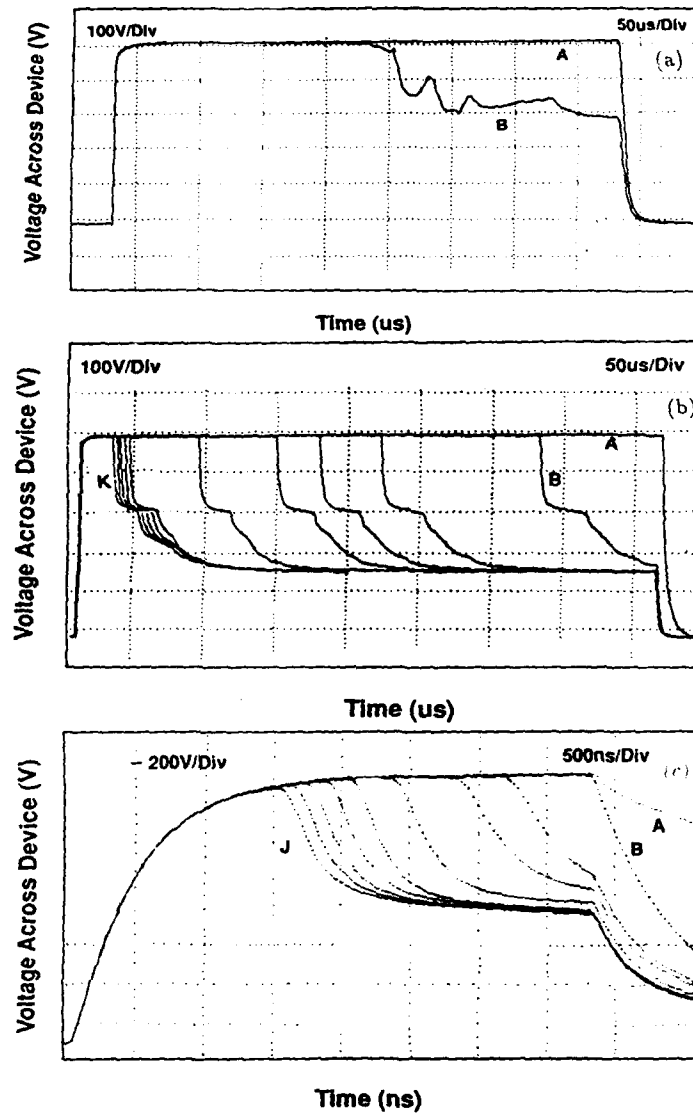


Fig.3 (a) Voltage across the bulk SI-GaAs device without (curve A) and with (curve B) a 10.5 mW LED illumination; (b) A negative -500V/400 μ s device bias voltage waveform (curve A) and the switching voltage across the optothyristor with LED illumination power at 0.01, 0.02, 0.04, 0.07, 0.2, 1.04, 1.28, 1.53, 1.77 and 2.00 mW (curves B through K); (c) A negative -1,300V/3.5 μ s device bias voltage waveform (curve A) and the switching voltage across the optothyristor with LED illumination power at 1.9, 2.5, 3.2, 4.4, 5.7, 7.0, 8.2, 9.3 and 10.5 mW (curve B through J).

Up to 2,200V forward bias has been applied to the device under pulsed condition and the switched current has been found to be up to 240A with a di/dt equal to 2.02×10^{10} A/s. The dynamic current-voltage characteristics at somewhat lower voltage level have been successfully recorded and are shown in Fig.4 where the time interval between the data points is 5 ns and the triggering light source has been replaced by the GaAs laser. It is seen in Fig.4 that at a forward bias of 1,450V the switched peak current is 56A which increases to 115A at 1,974V bias. There is always a very short, a few tens nanoseconds, delay time in the rising up of the switched current with respect to the switching of the voltage. This delay time appears to be due to the linear photoconductivity effects. But it is not clear to us why at 1,974V bias the photoconductive current persists for a long(almost 40 ns) time before the high current eventually picks up. We notice that switching delay time in GaAs homojunction optically triggered thyristors has been reported to be as long as more than 100 ns and has been explained by the regeneration process resulting from the feedback between the two transistors in the pnpn structure[11]. We do not yet have a good explanation about the increased delay time for the increased device bias, although it is possible to argue that the deep trap impact ionization coefficient may have a strong and nonlinear dependence on the field intensity such that a longer time is required at a higher field intensity to impact ionize the trapped carriers and to turn on the device completely which results in the high current peak.

If one can control this delay time the power consumption may be greatly reduced as can be seen in Fig.5 where the dissipated energy per switching has been determined and plotted as a function of device bias. The datum point for 1,974V bias has a lower energy dissipation because of a switching delay time of about 40 ns. Since Si based high power thyristors normally switch at a much slower speed, typically in the μ s range, it is expected that the fast switching of GaAs based optothyristors would dissipate much less energy and generate much less heat as shown in Fig.5. For the device operated at 1,974V with a 115A switched current the dissipated energy is less than 2 mJ. Notice that much larger percent of this 2 mJ energy will be dissipated by emitting photons through the direct band to band recombination in GaAs instead of in the form of heat or phonons when compared to that in Si thyristors.

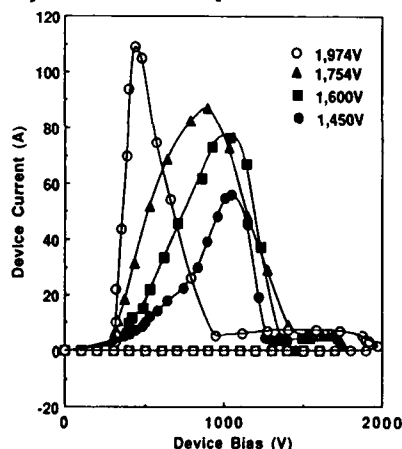


Fig.4 Forward dynamic I-V characteristics.

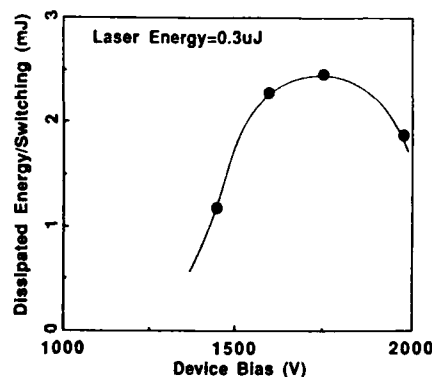


Fig.5 Dissipated energy per switching as a function of device bias.

Light-triggered thyristors are known to offer the best approach to HVDC thyristor valves and VAR-control switches of simpler design and to provide equipment designers simpler solutions to many application problems[12]. With SI-GaAs as the voltage blocking layer and the results shown in Fig.3 and 4, it is expected that by increasing the SI-GaAs thickness there is a great opportunity for GaAs optothyristors to outperform Si thyristors in the switching speed as well as the voltage and current ratings. Further experimental work is underway to fully understand and improve the device performance.

CONCLUSION

The first AlGaAs/GaAs heterostructure thyristor with bulk SI-GaAs as the voltage blocking layer has been demonstrated. The optically gated thyristor is capable of holding up to 2,200V(34 kV/cm) and switching 240A current with a di/dt equal to 2.02×10^{10} A/s if the surface of the device is passivated by LT-GaAs. The heavily doped wider band gap AlGaAs layers provide very good ohmic contacts and serve as optical windows for sensitive optical gating. The forward dynamic I-V characteristics have been studied and the dissipated energy per switching has been determined as a function of device bias. Reverse biased thyristor is found to be very interesting for pulsed switching applications because even an LED operating in the sub-mW range can turn on the switch. This makes it very attractive to integrate LED's with the thyristor on the same chip for triggering.

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PICOSECOND HIGH-VOLTAGE PULSES GENERATION USING LOW-TEMPERATURE (LT) GaAs

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ABSTRACT

We report on the generation of 825 V electrical pulses with 1.4 ps rise time and 4 ps Full-Width-at-Half-Maximum using pulse biased Low-Temperature-grown GaAs photoconductive switch triggered by submicrojoule, 150 fs laser pulses. Dependence of the temporal pulse shape on both the electric field and the optical energy is observed and discussed.

Introduction

In recent years many applications have emerged for high-voltage, high-speed switching.¹ Using photoconductive techniques both kilovolt switching and picosecond pulse generation have been achieved. High-voltage switching has been reported using high resistivity materials and high power lasers with large-dimension structures to achieve kilovolt switching. This resulted in pulses with duration down to 70 ps and rise time no less than 10 ps.² Conversely, high-speed switching has used short optical pulses with fast recovery time materials, small dimension structures and low power lasers to achieve generation of subpicosecond pulses with amplitude up to 6 V.^{3,4} To this day the competing needs of having a large gap to hold off high voltage and a small gap to maintain high speed have hitherto left kilovolt amplitude and single picosecond pulse generation decoupled.

The breakdown voltage or maximum bias voltage that can be applied to a photoconductive switch is determined by the dimension across which the bias is applied and the resistivity of the semiconductor material. This breakdown voltage may be increased by limiting the duration of the bias voltage. The fraction of bias voltage effectively switched depends on the energy of the optical pulse. The rise time of the electrical signal is determined by the duration of the optical pulse and by the switch bandwidth, which is a function of the switch dimensions. The pulse duration is limited by the carrier lifetime. Ultimately the geometry of the switch determines the maximum possible bias and the minimum rise time.

With conventional high resistivity GaAs or Si, the electric field hold-off is around 10^4 V/cm. Therefore, the small dimensions necessary for picosecond signal generation limit the applied voltage to few hundred volts. However, Low-Temperature-MBE-grown GaAs (LT-GaAs) has recently demonstrated extremely high resistivity and breakdown threshold.³ Furthermore, due to its subpicosecond carrier lifetime LT-GaAs satisfies the conditions for picosecond pulse generation. Using this material and the technique of pulse biasing, we have been able to apply up to 1.3 kilovolt to a 100 μ m switch making possible the generation of picosecond high-voltage pulses.

Experimental configuration

Efficient switching of kilovolt-level bias voltages requires an optical energy at the microjoule level, which necessitates the use of amplified laser pulses. Our laser (similar to that described in references 5 and 6) generates microjoule pulses at 620 nm at a 2-kHz repetition rate, using a two-stage dye amplifier pumped by a frequency doubled Nd:YAG regenerative amplifier. The laser pulse duration is 150 fs, ensuring that the picosecond electrical pulse generation and measurement are not limited by the optical pulse length.

A schematic diagram of the experimental configuration is shown in Figure 1. Pulse biasing is employed to prevent breakdown of the switch. Part of the frequency doubled Nd:YAG regenerative amplifier output is used to illuminate a dc-biased 4-mm-long

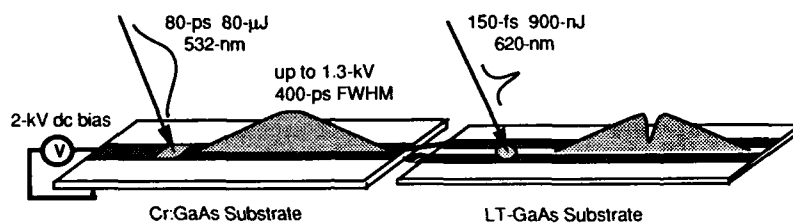


Figure 1: schematic of the experimental set up.

semi-insulating GaAs switch which is used as the pulse-bias network. The switch is mounted in a microstrip line geometry between a $\sim 10 \Omega$ charge line and a 90Ω transmission line. Illuminated by a $80 \mu\text{J}$, 80 ps optical pulse at 532 nm , this device produces an electrical pulse which has an amplitude equal to 70% of the dc bias voltage and a full-width-at-half-maximum of 400 ps . This pulse then biases a 90Ω coplanar stripline ($100 \mu\text{m}$ wide gold conductors separated by $100 \mu\text{m}$) on a LT-GaAs substrate. As the bias pulse propagates along the transmission lines, a 150 fs submicrojoule optical pulse illuminates the area between the lines. The high density of carriers formed within the LT-GaAs shorts the electrodes together. This technique of switching, known as "sliding contact", in principle allows total switching of the applied bias voltage.⁷ The resulting electrical waveform is schematically shown in Figure 1. External electro-optic sampling in a LiTaO_3 crystal with 150 fs , 100 pJ pulses is used to measure the signal $300 \mu\text{m}$ from the switch site.⁸ In our configuration the crystal has a half-wave voltage of $\sim 4 \text{ kV}$ ensuring a response linear within 2% over the range of voltages measured. The calibration error for the measurement is estimated to be 5% owing mainly to laser intensity fluctuations. Waveforms are recorded for different settings of bias voltage and illuminating energy. For convenience, the picosecond electrical waveforms are then extracted and displayed in a more conventional format.

Results

Figure 2 shows an 825 V pulse with duration of 4 ps and rise time of 1.4 ps . The negative precursor to the pulse is attributed to the radiation from the dipole formed at the generation site. For incident optical energies greater than 500 nJ we observe saturation of the switching efficiency, defined as the ratio of switched voltage to applied voltage, as shown in Figure 3. While the maximum switching efficiency is ideally 100%, the 70% experimentally measured can be explained by a combination of factors including radiation, dispersion and contact resistances.

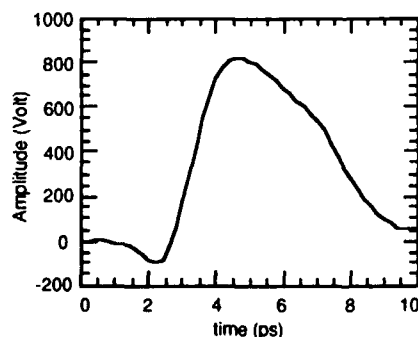


Figure 2: waveform showing a 825 V , 1.4 ps rise time and 4 ps duration pulse switched from a 1.3 kV bias with an optical energy of 900 nJ .

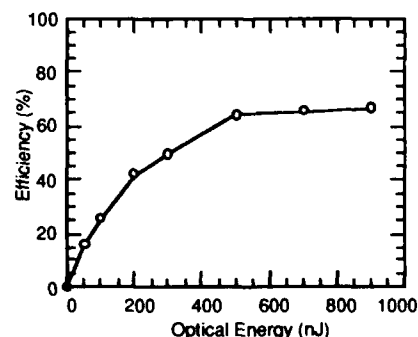


Figure 3: switching efficiency as a function of optical energy for an electric field of 100 kV/cm .

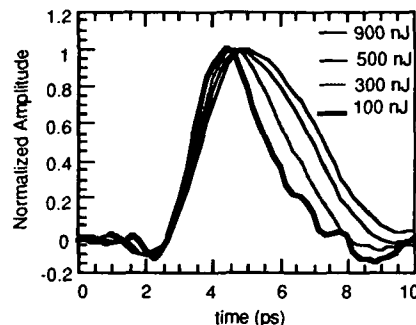


Figure 4: pulse shape as a function of optical energy for an electric field of 100 kV/cm.

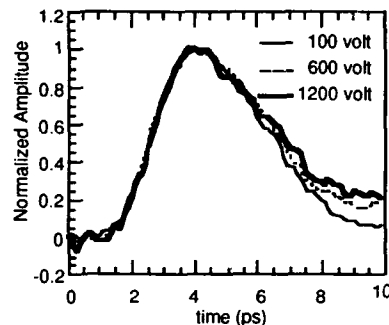


Figure 5: pulse shape as a function of applied bias for an optical energy of 900 nJ.

The rise time, ultimately limited by the 100 μm transmission line dimensions, reveals a clear dependence on the carrier density. As illustrated in Figure 4, we observe a degradation from 1.1 ps to 1.5 ps over the range of optical energy from 100 to 900 nJ. However, as shown in Figure 5, the rise time appears to be independent of the electric field. The relation of the rise time to the carrier density and the electric field is still not well understood. A possible explanation involves saturation of the available trapping centers. In LT-GaAs the short carrier lifetime is primarily attributed to arsenide precipitates acting as trapping centers. Under high carrier density the trapping centers could be saturated and the carrier lifetime would then become longer. This change in the carrier lifetime would affect the rise time as well as the duration of the electrical pulse. This explanation and others involving saturation of the current density and strong carrier scattering are presently being investigated.

Although a subpicosecond fall time was anticipated from previous measurements of LT-GaAs carrier lifetime,⁹ this experiment reveals a much longer recovery time. This tail increases as we increase either the carrier density or the applied electric field (Fig 4 and 5). Significant local heating due to the extremely high current densities (up to 10^7 A/cm^2) drawn through the switch area results in generation of additional carriers and could explain this long recovery time, however it does not account for the rise time degradation. In the following, we present another possible justification for the long recombination time, involving intervalley scattering which is known to be strongly dependent on both the electric field and the carrier density.

The switched electrical pulse shape reflects the evolution of the current density, which is proportional to the product of carrier density and average carrier velocity. A carrier's contribution to the switching process is then proportional to its velocity. In GaAs, a photogenerated hot electron under a strong electric field can scatter from the central valley to the high-effective-mass satellite X- and L-valleys, greatly reducing its velocity and therefore its contribution to switching. The scattering probability increases with the electrical field and, under our experimental conditions, we estimate that more than 80 % of the carriers are in the satellite valleys after 100 fs.¹⁰ The transfer of those electrons back into the central valley occurs on the picosecond time scale.¹¹ The probability of transfer into a specific valley is a function of the density of available states in this valley, therefore as the pump energy increases the carrier density in the central valley rises. Consequently, the probability for an electron to scatter back into the central valley decreases. As the carriers still in the high mobility valley recombine (within few hundred femtoseconds for LT-GaAs), the probability to transfer back from the satellite valleys increases with time. The satellite valleys can then be seen as sources reinjecting hot electrons into the central valley at a rate dependent on the relative carrier populations which are function of optical fluence, electric field, and wavelength.

Summary

In conclusion, we report on the application of LT-grown GaAs for photoconductive switching using a pulse bias technique leading to the generation of an 825 V pulse with 1.4 ps rise time

and duration of 4 ps. This represents the highest voltage ever obtained in the single-picosecond time scale. This new capability to produce ultrashort high peak power pulses could be of interest for applications in fields such as millimeter-wave non linear spectroscopy, radar signal generation, source for linear accelerator of particles and ultrafast instrumentation. Future work will include spectroscopic studies to determine the carrier dynamics and populations during the switching process.

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MULTI-HUNDRED GIGAHERTZ PHOTODETECTOR DEVELOPMENT USING LT GaAs

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ABSTRACT

We report on the development of a new, integrable photoconductive-type detector based on low-temperature-grown GaAs. The detector has a response time of 1.2 ps and a 3-dB bandwidth of 375 GHz. The responsivity is 0.1 A/W. This is the fastest photodetector reported to date. We discuss the unique properties of this device, including its performance as functions of both light intensity and bias voltage.

INTRODUCTION

Much progress has been made over the past several years in the development of high-speed photodiode detectors. A detection bandwidth of 105 GHz together with a responsivity of 0.1 A/W have been reported for a metal-semiconductor-metal (MSM) photodiode.[1] The most common approach to increasing the bandwidth in MSM photodiodes (at least up to 100 GHz) is to shorten the carrier transit time by reducing the electrode spacing. However, achievement of bandwidths > 100 GHz requires more than simply reducing further the electrode spacing. Monte Carlo simulation of the intrinsic response for a photodiode with 0.1- μ m electrode spacing, for example, shows a response tail persisting for picoseconds and having an integrated energy comparable to the main signal.[2,3] This tail is caused by the long transit time of the photogenerated holes, which is almost 10 times that of electrons.

The response times of photoconductive detectors, on the other hand, can be quite fast because they are determined solely by the carrier lifetime of the material that is used. Recently, low-temperature-grown GaAs (LT GaAs) has been applied to ultrafast [4] and high-power [5] optical switching. The subpicosecond carrier lifetime,[6] high mobility (> 200 cm²/V·s), and high breakdown field strength (>100 kV/cm) of LT GaAs make this material ideal for electrical pulse generation and gating. Such applications have so far required use of moderate-to-high peak optical powers since the switching efficiency, defined as the ratio of electrical output power to optical input power, is still < 1%. However, as we have found, the switching efficiency tends to be influenced more by the electrode dimensions than by the intrinsic characteristics of the material.

We now report a LT GaAs-based photoconductive detector that takes advantage of the high breakdown field capability of LT GaAs to greatly improve sensitivity. In a photodiode, a reduction in electrode spacing improves speed with little change in sensitivity. In a photoconductive detector, by contrast, such a reduction increases the sensitivity with little change in speed. Decreasing the carrier transit time across the semiconductor gap to a value comparable to the

carrier lifetime increases the photocurrent gain to a value of unity.[7] For a carrier lifetime of 1 ps, this condition is met when the electrode spacing, i.e., the actual gap between electrodes, is 0.1 μm . A further decrease in the electrode spacing could increase the photoconductive gain to an even higher value, provided the metal-semiconductor contacts are ohmic. With unity gain, the responsivity of a LT GaAs photoconductive detector becomes comparable to that of a photodiode, while its speed is still dominated by the (sub)picosecond intrinsic carrier lifetime.

EXPERIMENT

To demonstrate this principle, we fabricated a LT GaAs photoconductive detector with interdigitated electrodes having finger widths and spacings of 0.2 μm , as shown in Fig. 1. A 1.5- μm -thick LT GaAs layer was grown on a (100) semi-insulating GaAs substrate that has a 0.4- μm -thick conventionally grown undoped buffer layer. The LT GaAs layer growth was performed using molecular beam epitaxy at a substrate temperature of 190 $^{\circ}\text{C}$, followed by annealing at 600 $^{\circ}\text{C}$ for 10 min in an arsenic overpressure. The interdigitated electrodes were fabricated of 300- \AA /2000- \AA Ti/Au using a JEOL JBX 5DIIF direct-write electron-beam lithography system. The active area of the detector is $6.5 \times 7.6 \mu\text{m}^2$. Coplanar transmission line electrodes of 500- \AA /2500- \AA Ti/Au, with 20- μm widths and spacings and 5-mm lengths, were also fabricated on the LT GaAs using conventional optical lithography. For comparative purposes, similar structures were also fabricated with 1.0 μm finger spacings and width.

Referring to Fig. 1, the LT GaAs photoconductive detector was placed between coplanar transmission lines ($Z_0 = 90 \Omega$) to assure good coupling of the generated electrical pulse to the propagating mode and also to eliminate parasitic losses. The detector was not antireflection (AR) coated in this initial work. A reference transmission line of identical dimensions, but without the interdigitated-electrode detector, was also fabricated on the wafer to determine the system response. The technique of sliding-contact switching, which provides the excitation between the lines without the interdigitated-electrode detector, can have a response < 0.5 ps.[8] The photoconductive detector was characterized using the technique of external electrooptic (EO) sampling [6]. A balanced, colliding-pulse, mode-locked dye laser operating at 610 nm with a repetition rate of 100 MHz was used, which produces 150-fs pump and probe pulses. The electrical signal was measured on the transmission line at a distance of 450 μm from the detector. Although not shown in the figure, the EO sampling crystal spanned both the detector/transmission-line assembly and the reference transmission line, so that the translation of the pump and probe beams required to make either measurement was only $\sim 200 \mu\text{m}$.

RESULTS AND DISCUSSIONS

A bias of 10 V dc was applied to the detector before breakdown occurred, corresponding to a breakdown field strength of 500 kV/cm. This value is more than twice the highest that has been reported for LT GaAs under dc-bias conditions, which was obtained using 20- μm -spaced electrodes.[9] Our result represents a better measurement of the actual breakdown field strength for LT GaAs, since our 0.2- μm electrode spacing confines the electric field to the 1.5- μm -thick LT GaAs epilayer. The dark current for 1 V applied to the detector is 100 pA. At 8 V (400 kV/cm), where we chose to operate, the dark current increased to 300 nA. For an average optical power of 4 μW , the responsivity is 0.1 A/W. Past work using 20- μm -spaced electrodes on LT GaAs attained a

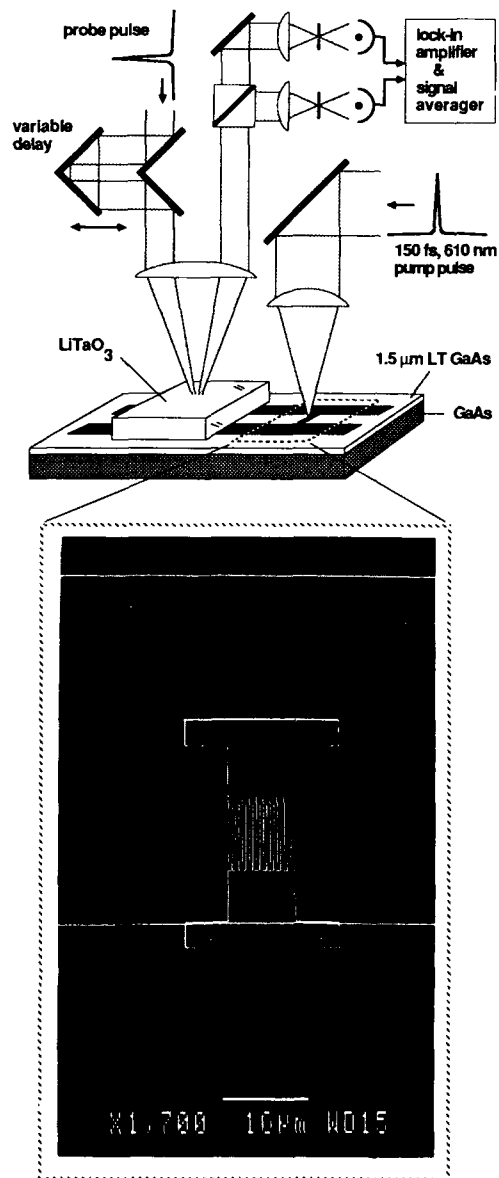


Figure 1. Photoconductive-type detector based on low-temperature-grown GaAs. The width and spacing of the interdigitated electrodes are $0.2\ \mu\text{m}$. The detector is fabricated across $20\text{-}\mu\text{m}$ width/spacing coplanar striplines to minimize parasitic effects.

responsivity of only 10^{-3} A/W.[9] The 100-fold reduction in gap dimension therefore improves the responsivity 100 fold. The value of 0.1 A/W is comparable to that for the responsivity of high-speed photodiodes. The reflective losses at the surface from the interdigitated electrodes and the semiconductor amounted to 70% of the incident signal, for an internal quantum efficiency of 68%.

The intrinsic material response time for the LT GaAs sample has been measured previously using an all-optical pump-probe technique [10] and found to be 0.6 ps. We calculate the capacitance [11] of our structure to be 4 fF, for an RC-limited response time of 360 fs. Fig. 2a shows the measured responses for the detector/transmission-line assembly and the sliding-contact switch on the reference transmission line. Both measurements were obtained 450 μ m from the point of signal generation. The optical pulse energy on the detector is 0.04 pJ (4- μ W average power).

The full-width-at-half-maximum of the detector response is 1.2 ps with no evidence of a tail. In fact, the trailing edge, with a 10-90% fall time of 0.8 ps, is faster than the leading edge. We note a similar shape of the response for the sliding-contact switch on the reference transmission line. This is indicative of modal dispersion from quasi-TEM propagation along a transmission line having a substrate and superstrate with different permittivities.[12] Since the measured results are a convolution of the LT GaAs intrinsic response time and such system-related factors as the RC time constant, laser pulse width, and electrooptic material response, the intrinsic response time for the interdigitated-electrode detector may in fact be subpicosecond. The -3-dB point for both signals occurs at 375 GHz, measured by taking their discrete Fourier transforms. A set of waveforms for several values of pulse energy is shown in Fig. 2b. The four signals have peak amplitudes of 0.06, 0.6, 3.5, and 6 V generated using 0.04, 0.83, 8.3, and 22 pJ/pulse respectively. A pulse energy of 22 pJ corresponds to an

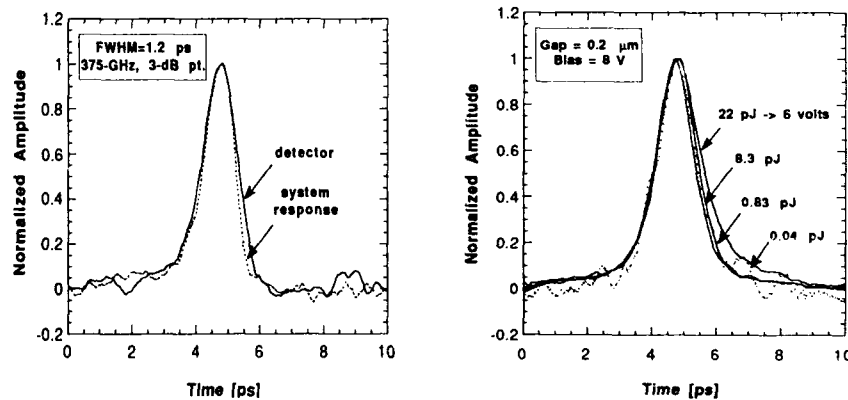


Figure 2. (a) Temporal response of the photoconductive detector and sliding-contact switch measured 450 μ m from the point of signal generation. The -3-dB point for both signals occurs at 375 GHz. (b) Set of four traces corresponding to peak signal amplitudes of 0.06, 0.6, 3.5, and 6 V generated using 0.04, 0.83, 8.3, and 22 pJ/pulse respectively.

on-state resistance of $30\ \Omega$. We see that a nearly 500-fold increase in intensity expands the response only slightly from 1.2 to 1.5 ps. Under similar experimental conditions, a high-speed photodiode would suffer significant temporal broadening from space charge [13] and from low-frequency gain by photoinduced band bending.[14] Thus, the LT GaAs photoconductive detector avoids the usual restriction of photodiodes to pulse energies below 0.1 pJ.

In Fig. 3a we show the electric-field dependence for the $0.2\ \mu\text{m}$ detector. Measurements were made with electric field strengths of $25\ \text{V}/\mu\text{m}$, $15\ \text{V}/\mu\text{m}$, and $5\ \text{V}/\mu\text{m}$. We see that there is little change in the pulse width, and in particular, the decay time with electric field. A similar measurement was carried out for the $1.0\ \mu\text{m}$ detector, as shown in Fig. 3b. Here, we see a noticeable increase in decay time with an electric field as low as $10\ \text{V}/\mu\text{m}$. One possible explanation for the gap dependence on decay time involves the process of impact ionization.[15] When the electric field exceeds a certain value, photoinduced carriers can accelerate to an energy large enough to ionize additional carriers. The occurrence of impact ionization will increase the decay time. The rate of ionization is dependent on both the electric field and electrode spacing. The field in both structures is well above the threshold value for impact ionization. However, the much shorter electrode spacing, in the case of the $0.2\ \mu\text{m}$ structure, prevents the process from fully developing.

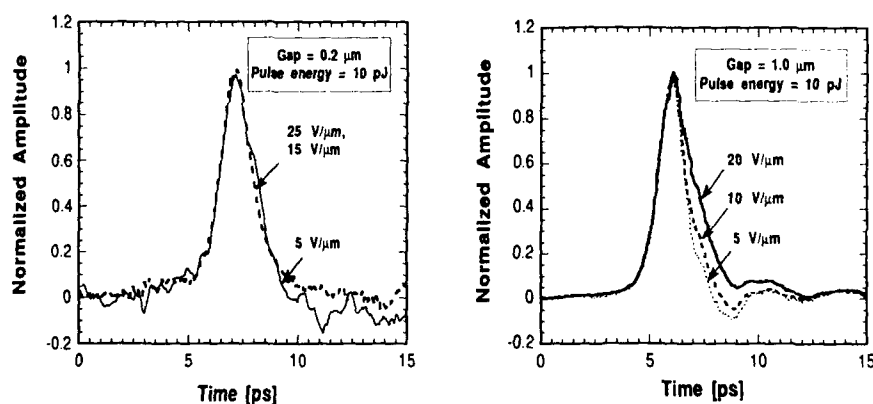


Figure 3. The LT-GaAs photoconductive response as a function of electric field. (a) with electrode width and spacing of $0.2\ \mu\text{m}$, (b) with electrode width and spacing of $1.0\ \mu\text{m}$.

In conclusion, we have developed a new MSM-type photoconductive detector, based on low-temperature-grown GaAs, fabricated using $0.2\text{-}\mu\text{m}$ -spaced interdigitated electrodes. The response time measured directly by EO sampling, i.e., without deconvolution, is 1.2 ps. With no AR coating on the detector, the responsivity is $0.1\ \text{A/W}$. To our knowledge, this is the fastest high-sensitivity photoconductive detector of any kind reported to date. In addition, it can be driven to an on-state resistance of $30\ \Omega$ with little degradation in speed. This versatility permits the device to function both as a detector and a switch. In the switching mode, the device can perform either as a high-contrast gate with a

picosecond gate window or as an efficient single-picosecond electrical-pulse generator. Such unique dual functionality together with ease of integration will permit a number of detector elements to be combined for acquiring and processing picosecond optical and electrical events with high efficiency and minimal temporal distortion.

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LONG WAVELENGTH CHARACTERIZATION OF INTERNAL QUANTUM EFFICIENCY IN LT-GaAs MSM PHOTODIODES

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ABSTRACT

Metal-Semiconductor-Metal (MSM) photodiodes fabricated from low temperature (LT) grown GaAs by molecular beam epitaxy have been characterized for wavelengths extending out to 1.5 μm . External quantum efficiencies on the order of 0.5 % have been measured for sub-bandgap wavelengths, which translates to internal quantum efficiencies of 2-4 % for the interdigitated electrode structure with 1 μm finger spacing and width. Although the effective lifetime of the LT-GaAs has been determined to be <1ps, an MSM photodiode response of ~10ps full width at half maximum was measured by correlation techniques at 820 nm wavelength, and a system limited response of 3GHz was measured at 1.3 μm wavelength. These experimental results will be described in detail.

INTRODUCTION

GaAs grown by MBE at low substrate temperatures (LT-GaAs) has previously demonstrated photoconductive devices having subpicosecond response times measured by electro-optic sampling [1] or detection of femtosecond pulses of terahertz radiation [2]. It has been determined that the predominant defects which provides for fast capture of photogenerated carriers are arsenic precipitates which form as a result of diffusion by the excess arsenic in the epitaxial layer during thermal annealing at temperatures ranging from ~580°-850° C. Depending on the particular growth conditions, anneal temperature and time, the precipitates will have diameters and spacings ranging from 2-50 nm [3]. The GaAs between the As precipitates is unstrained and has high crystalline quality. It is believed that these precipitates are metallic in nature contacting the GaAs crystal lattice as a Schottky barrier [4], although alternative models based on deep level trapping states cannot be ruled out. As a result of the large concentration of efficient capture centers for photogenerated charge in the LT-GaAs, it provides an excellent material for picosecond photodetectors. More recently, interdigitated MSM photodetectors having 2000Å finger spacing and widths fabricated on LT-GaAs have been reported [5], providing the best responsivity-bandwidth performance to date. It has also been observed that LT-GaAs exhibits measurable absorbance in the sub-bandgap wavelength regime, and reports of photodetector performance at 1.3 μm wavelengths have recently been presented [6]. Although the responsivity of LT-GaAs photodetectors at wavelengths beyond 1 μm is nowhere near comparable to that of above bandgap wavelengths, these results provide some interest in that a GaAs based photodetector for long wavelengths would enable the integration of high performance GaAs signal processing circuitry. The objective is to optimize the LT-GaAs photodetector performance at long wavelengths.

LT-GaAs MSM PHOTODIODE FABRICATION

Metal-semiconductor-metal (MSM) photodiodes have been fabricated on LT-GaAs epitaxial layers. The material was grown by MBE at a "calibrated" substrate temperature of 190° C using an As₄ source with a Group V to III beam equivalent pressure ratio of ~12. The layer was grown at a nominal growth rate of 0.8-0.9 $\mu\text{m/hr}$ to a thickness of 2 μm . The post growth anneal consisted of a 620° C thermal cycle for 20 minutes. The resulting LT-GaAs had a high

density of arsenic precipitates ($\sim 3.5 \times 10^{15} \text{ cm}^{-3}$) with diameters on the order of 90 Å and spacings of approximately 200 Å. The GaAs between the precipitates is unstrained and of extremely high quality as observed by Transmission Electron Microscopy (TEM). Interdigitated fingers for the MSM structure having 1 μm width and spacing, and 50 μm lengths were defined by photolithography. Subsequent metal deposition consisted of Ti/Pt/Au (300Å/300Å/1000Å) after which the photoresist was lifted off by acetone to complete the process. MSM photodiodes were fabricated in correlation circuits as illustrated in Figure 1 in order to measure the transient response on-chip before being distorted by the transmission line structure, bond wires, and external contacts. This enables temporal resolution on the order of 1 ps. The I-V characteristics of the MSM photodiode is shown in Figure 2, demonstrating dark leakage current in the 10^{-9} A range up to several volts bias.

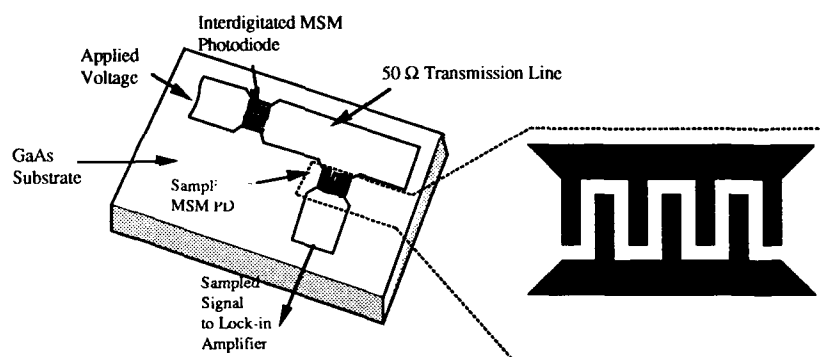


Figure 1: LT-GaAs Metal-Semiconductor-Metal photodiode structure and correlation circuit.

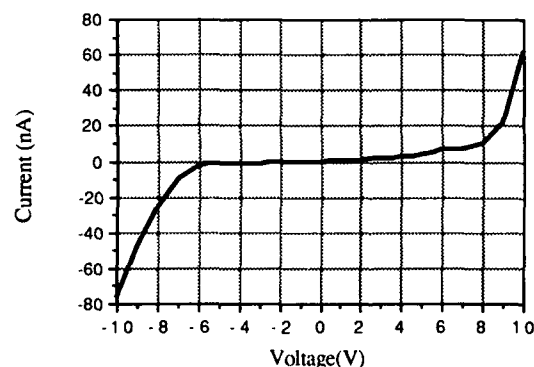


Figure 2: Dark I-V characteristics of LT-GaAs MSM photodiode with 1 μm finger spacings.

EXPERIMENTAL RESULTS

The room temperature spectral response of the LT-GaAs MSM photodiodes described above was measured over the 0.8 to 1.5 μm wavelength range using a calibrated spectrometer source. The external quantum efficiency as a function of wavelength is illustrated in Figure 3.

From these results, external quantum efficiencies on the order of 0.5% were observed for wavelengths from 1.0 to 1.5 μm , where it begins to roll off. Since the interdigitated electrodes cover 50% of the detector area, and the reflectivity of the GaAs surface is approximately 34 %, this corresponds to an internal quantum efficiency of $\sim 2\text{--}4\%$.

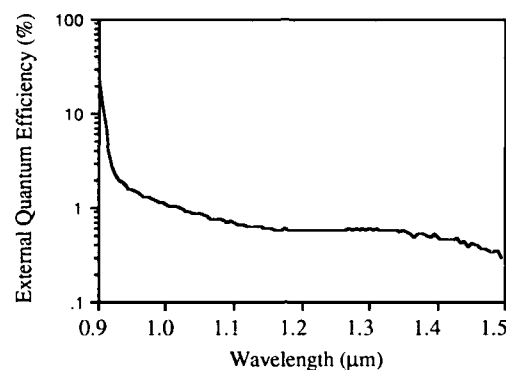


Figure 3: Spectral dependence of external quantum efficiency for LT-GaAs MSM photodiode.

The temporal response of the LT-GaAs MSM photodiodes was measured by correlation techniques. The optical source used here is a synchronously pumped dye laser which produces 700 femtosecond full width at half maximum (FWHM) pulses at 820 nm wavelength. The photocurrent response of the MSM photodiode to the incident optical pulse is launched onto a transmission line which is then sampled by the second MSM photodiode. By varying the relative time delay of the optical pulses between the pulsing and sampling photodiodes, the cross-correlation response of the MSM photodiode is measured, which can be deconvolved to determine the actual response. These results are shown in Figure 4. Deconvolving this response gives a pulse width of ~ 10 ps FWHM. The transient response of the LT-GaAs MSM photodiode is probably limited by the capacitance of the interdigitated electrode structure since the carrier lifetime has independently been measured to be less than 1 ps [7].

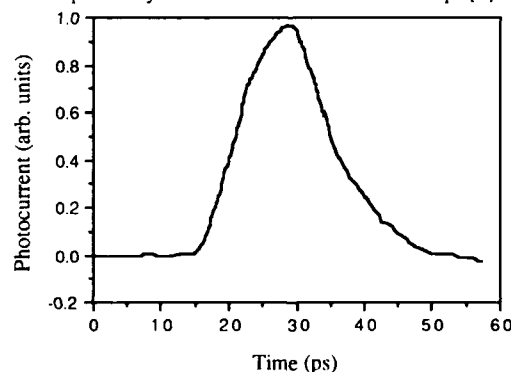


Figure 4: Cross-correlation response of LT-GaAs MSM photodiode.

The photocurrent response of LT-GaAs MSM photodiodes was also characterized at 1.3 μm wavelength. Photocurrent-voltage characteristics with 25 mW of 1.3 μm light are illustrated in Figure 5. From this the responsivity is determined to be ~ 3 mA/W for cw power. The experimental setup shown in Figure 6 was utilized to characterize the modulated response at

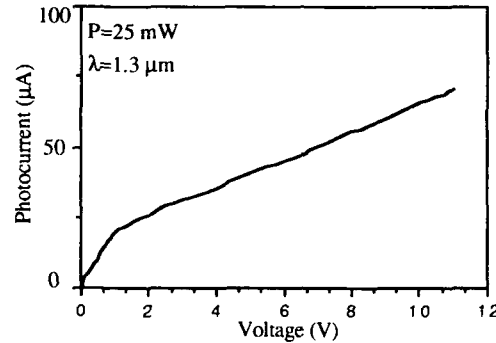


Figure 5: Photocurrent-voltage characteristics at 1.3 μm for LT-GaAs MSM photodiode.

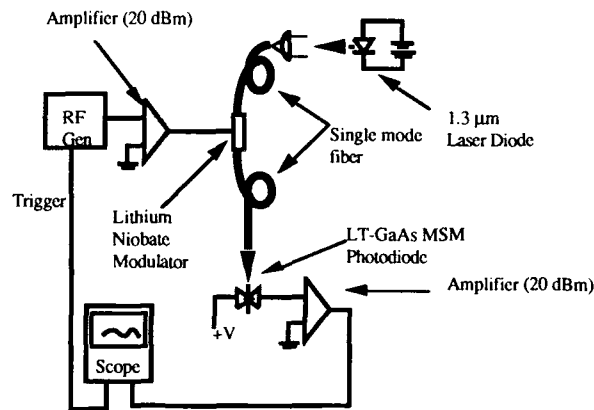


Figure 6: Setup for testing LT-GaAs MSM photodiode modulation response at 1.3 μm .

1.3 μm . Lithium Niobate Mach Zender interferometers were utilized to modulate the cw optical signal. The output of the MSM photodiode was amplified 20 dBm and displayed on a sampling oscilloscope. Figure 7-a,b illustrate the input rf signal and modulated response of the LT-GaAs MSM photodiode for this experiment. The response is limited to 3 GHz by the experimental setup.

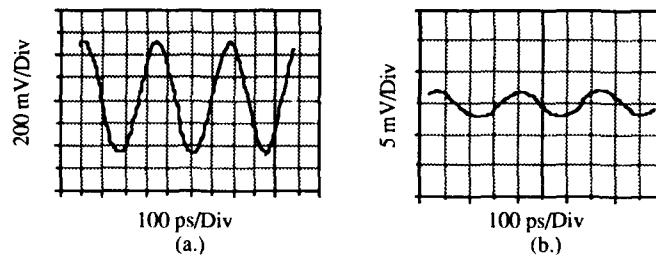


Figure 7: a.) 1.3 μm modulation signal and b.) LT-GaAs MSM photodiode response.

CONCLUSION

LT-GaAs MSM photodiodes with 1 μm finger spacing and width have been fabricated and tested. The measured photocurrent spectra demonstrates ~2-4% internal quantum efficiency over the 1.0-1.5 μm wavelength regime, and a calibrated responsivity of 3 mA/W at 1.3 μm . Although these photodiodes have demonstrated high frequency response at 820 nm and 1.3 μm wavelengths, further improvements can be realized through better electrode design, and improved experimental setup. This offers the possibility of an entirely GaAs-based 1.3 μm receiver circuit.

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LASER QUALITY AlGaAs-GaAs QUANTUM WELLS GROWN ON LOW TEMPERATURE GaAs

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ABSTRACT

In this work we demonstrate that photopumped quantum well heterostructure lasers with excellent optical quality can be grown on top of a LT GaAs buffer layer by molecular beam epitaxy. High temperature thermal annealing of these lasers blue-shifts the laser emission wavelengths but the presence/absence of a LT GaAs layer had little effect on the overall laser thresholds. Also, to first order it was not necessary to include an AlAs barrier layer to prevent adverse effects (as has been necessary in the gate stack of MESFETs to prevent carrier compensation).

INTRODUCTION

Low temperature GaAs (LT GaAs) grown by molecular beam epitaxy (MBE) at a low substrate temperature of 200°C and subsequently *in situ* annealed at high temperatures (600°C, for example) has been shown to be highly resistive and optically inactive. These properties are attributed to a combination of excess arsenic and a large quantity of antisite defects [1,2]. Despite its seemingly undesirable electrical and optical properties, LT GaAs has been used in GaAs MESFETs [3,4], GaAs based HEMTs [5], photodetectors [6] and optical switches [7]. When LT GaAs is used as an insulator under the gate or as a buffer layer in MESFET structures, some adverse effects associated with the subsequent high temperature *in situ* anneal occur [8]. A thin AlAs layer has been shown to prevent these adverse effects by preventing the outdiffusion of excess arsenic related defects in the LT GaAs [8].

EXPERIMENTAL

The separate confinement single quantum well heterostructures (SCSQWH) used in this study were grown by MBE (Varian 360) on

undoped semi-insulating (100) oriented GaAs substrates. The SCSQWHs were grown by first depositing buffer layer(s) and then an $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ - $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ -GaAs separate confinement heterostructure as shown in Figure 1. Two sets of samples were prepared to: 1) compare a regular GaAs buffer to a LT GaAs buffer, and; 2) to compare regular GaAs to LT GaAs both with a 200Å AlAs layer. The LT GaAs layer was grown at 200°C and *in situ* annealed at 590°C for 10 minutes under arsenic overpressure prior to deposition of the subsequent layers.

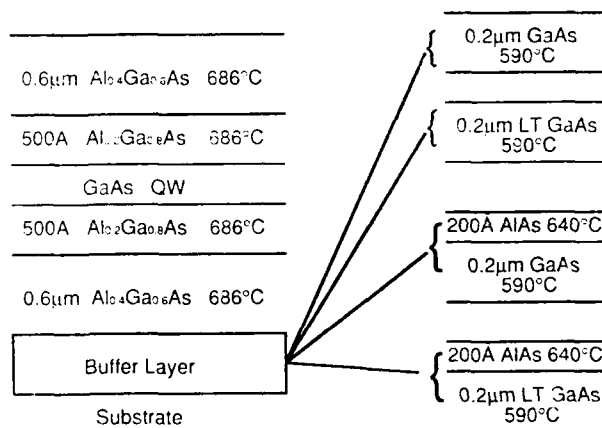


Figure 1: Schematic cross section of the SCSQWH laser samples with four different buffer layers grown by MBE.

Post growth annealing was done in sealed quartz ampoules evacuated to 10^{-6} Torr with sufficient arsenic (5mg) to provide an arsenic overpressure of approximately 0.1 atmosphere in the range from 650-900°C. Laser samples were prepared by selectively removing the substrate from the epilayers, cleaving the remaining film into rectangular platelets 20-100 μm in width, and pressing the platelets into indium under a sapphire window. Photoexcitation was achieved by focusing light from a cavity-dumped argon-ion laser ($\lambda = 5145\text{\AA}$, 8ns pulses at 3.8MHz). Luminescence from the samples

was collected and analyzed using a 0.5-m spectrometer and S-1 photomultiplier.

RESULTS AND DISCUSSION

The objective of this work was to determine if laser quality AlGaAs-GaAs could be grown on top of LT GaAs, and if so, would the outdiffusion of arsenic related point defects from the LT GaAs have an adverse impact on the lasers. Laser spectra (77K) from the samples without the AlAs barrier layer are shown in Figure 2. Note

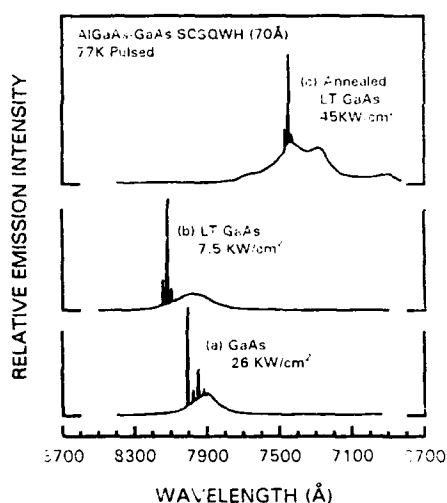


Figure 2: Stimulated emission spectra from SCSQWH laser samples prepared as cleaved platelets. Spectrum (a) from the sample with a regular GaAs buffer layer; (b) with a LT GaAs buffer layer; and (c) from the post-growth annealed (900°C, 3 hrs.) sample with a LT GaAs buffer layer.

that the GaAs control sample, the LT GaAs sample and the annealed (900°C, 3 hours) LT GaAs sample all operated as photopumped lasers. The photopumped power densities are high compared to current injection lasers because of the short cavity length of the platelets (10-50μm) compared to laser diodes (250-500μm). Also, the power densities given in the figures correspond to the experimental conditions not the laser threshold densities. Laser spectra from the samples with the AlAs layer are shown in Figure 3. Again, laser operation was achieved for all three experimental conditions. Laser

thresholds vary from one platelet to another (due to cavity effects and nonuniform pumping) but on average there was little difference in performance regardless of the buffer layer or inclusion of an AlAs layer. This indicates that it should be possible to fabricate high quality injection lasers on top of LT GaAs.

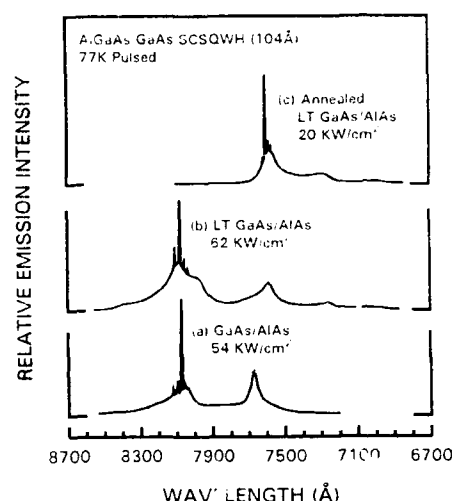


Figure 3: Stimulated emission spectra from SCSQWH laser samples prepared as cleaved platelets. Spectrum (a) from the sample with a regular GaAs/AlAs buffer layer; (b) with a LT GaAs/AlAs buffer layer; and; (c) from the post-growth annealed (900°C, 3 hrs.) sample with a LT GaAs/AlAs buffer layer.

One measurable difference between the GaAs and LT GaAs buffer layer samples was the degree to which the post-growth annealed sample emission was blue shifted. The blue shift is due to the intermixing of the AlGaAs-GaAs quantum well interface [9] and the Al-Ga interdiffusion coefficient can be determined based on the shift of the quantum well luminescence [10]. The samples were annealed in sealed ampoules under arsenic overpressure for 4 hours at temperatures ranging from 650-925°C. Photoluminescence spectra from all of the samples had comparable intensities and full widths at half maximum. There was very little blue shift for samples annealed for four hours in the temperature range from 650°C to 800°C. This indicates that the excess arsenic related defects are either stable in this temperature range or did not reach the quantum well in sufficient numbers to enhance intermixing. However, at 850°C the samples with LT GaAs buffer layers (with or without AlAs) exhibited

substantially increased intermixing. The Al-Ga interdiffusion coefficient for a GaAs quantum well on top of different buffer layers [11] is shown in Figure 4. The additional solid points are the interdiffusion coefficients for the laser samples in this study. Note in all cases that the LT GaAs buffer layer enhances the solid state intermixing of the GaAs quantum well with the AlGaAs confining layers. The absence of additional data points at higher temperatures is because the intermixing of the QW with the $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ confining layers can not be distinguished from the intermixing caused by the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ cladding layers (at higher temperatures).

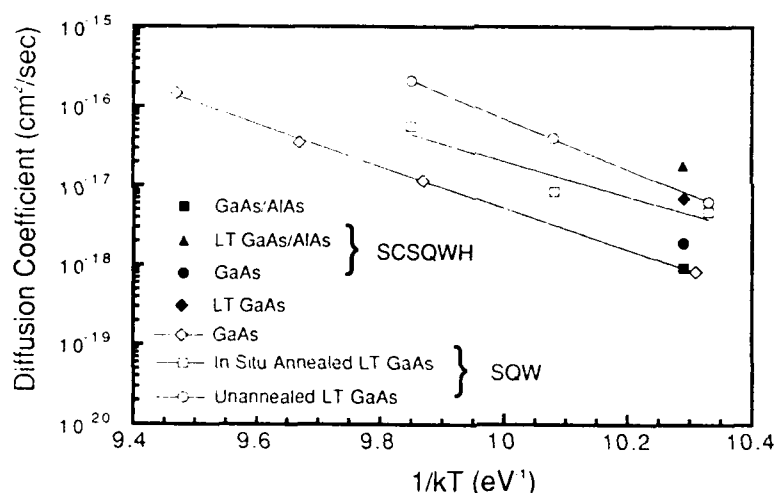


Figure 4. Plot of the interdiffusion coefficient of the Al-Ga atoms under As overpressure as a function of $1/kT$. The open data points are from reference [11]. The solid points correspond to the SCSQWH samples with different buffer layers as shown in Figure 1.

CONCLUSIONS

Laser quality AlGaAs-GaAs quantum wells can be grown on top of a LT GaAs buffer layer. Post growth annealing blue shifts the quantum well luminescence energy more rapidly in samples with a LT GaAs buffer layer. The accelerated intermixing is attributed to Ga

vacancies associated with the excess arsenic in the LT GaAs. The inclusion of a 200Å thick AlAs barrier layer did not impact the laser performance or intermixing of the quantum wells. Laser operation was observed from all the as-grown and annealed samples. The prospect of using LT GaAs as an isolation layer for electrical and optical devices in integrated optoelectronic circuits is quite promising.

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MOLECULAR BEAM EPITAXY OF LOW TEMPERATURE GROWN GaAs PHOTOCONDUCTORS

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ABSTRACT

We report on the characterization of Low Temperature (LT) epitaxial growth of GaAs photoconductors. Samples were characterized using electro-optic sampling, transient femtosecond reflectivity, transmission electron microscopy, and pulsed terahertz spectroscopy as a function of growth temperature, As₄ flux, doping and anneal conditions. We find the strongest effect on pulsewidth to be the *temperature* of an ex-situ rapid thermal anneal. In addition we find evidence of a *temperature threshold* for As precipitation. For more than an order of magnitude change in As precipitate density we find no corresponding change in electrical pulsewidth. Doping to $10^{17}/\text{cm}^3$ also produces no change in the measured electrical response.

INTRODUCTION

Short carrier lifetime semiconductors are an important component of an ultrafast *electrical* characterization system. Intrinsic GaAs, when used in conjunction with a fast, sub hundred femtosecond FWHM (Full Width at Half Maximum) laser pulse, produces carrier populations with subpicosecond rise times, but hundred picosecond fall times. Usually, a transmission line structure is formed by metal electrodes with some sort of gap forming the switch, with one side biased, and the other acting as the output line. This structure, when illuminated by a short optical pulse transforms the *optical* pulse into an *electrical* pulse. The electrical pulse is limited, in general, not by the optical pulse, but by the carrier population which produces the electrical transient.

The long fall time associated with intrinsic GaAs can introduce complicated electrical reflections. Ideally, one would wish for a delta function, large in amplitude, and with vanishing temporal width, so that spectral analysis would be clean and simple, and a device integrable with other active and passive components. While damaged Si on Sapphire (SOS) provides pulses with very narrow temporal width, satisfying the first requirement, their amplitude is very small, typically only a few mV. In addition SOS devices are not easily integrable with GaAs devices.

The first LT grown GaAs photoconductors [1] produced pulses about 1.5 ps FWHM, but it was clear that this technology offered the possibility of both large amplitude, and short pulsewidth in an integrable technology.

In this paper we present the first in depth study of LT GaAs photoconductors. While short pulsewidths have been realized [2], there has been no systematic study of pulsewidth with respect the myriad of variables involved in the MBE growth and subsequent annealing processes.

GROWTH

Sample histories, as well as a summary of some of the characterization results are shown in Table 1. Growth was carried out in a UHV MBE chamber with a base pressure of $<10^{-11}$ Torr and a peak pressure during deposition of $<10^{-10}$ Torr. The sources were elemental Ga and (uncracked) As Knudsen cells, and growth rates were typically in the region of $1\text{-}4\text{\AA}/\text{s}$. Clean GaAs surfaces were prepared by growth of 500\AA - $1\mu\text{m}$ of GaAs at high temperature ($500\text{-}600^\circ\text{C}$) on nominally (100) substrates

following a standard cleaning procedure. The substrate was then cooled to the desired low temperature and allowed to reach equilibrium prior to deposition of a thick (typically 0.5 μm) LT GaAs layer. Substrate temperatures were measured using optical pyrometry at high temperature and a calibrated thermocouple attached to the substrate heater at temperatures below $\sim 500^\circ\text{C}$. Thus although relative temperatures should be accurate to within $\pm 5^\circ\text{C}$ even for $T < 500^\circ\text{C}$, the absolute values quoted in this paper are only reliable to within $\pm 25^\circ\text{C}$. Two different MBE chambers were used to produce material, and *both* ultimately produced sub-ps pulsewidths. Growth thicknesses was chosen to be less than the epitaxial thickness, beyond which amorphous growth occurs [3].

Table I. Summary of LT GaAs results

Sample	Density of As $10^{16}/\text{cc}$	Volume Fraction (10^{-4})	E/O Pulse Width (ps FWHM)	Growth Temp. ($^\circ\text{C}$)	Anneal Temp. ($^\circ\text{C}$)	Anneal Time (min)	As ₄ Flux	Doping $10^{17}/\text{cc}$
91206			1	277	500	15	1.4	none
91207			1	287	500	15	1.4	none
91208			1	287	500	15	1.4	1
91178	21	2	1.35	307	600	15	2	none
91179	9	2	1.05	307	600	15	2	none
91168	19	10	1.25	287	600	5	1	none
91167	28	3	1	307	600	5	1.4	none
91166	30	3	1	307	600	5	2	none
91088	13	1	1.05	307	600	5	1	none
1108905	16	20	0.78	327	600	5	1	none
918911	120	10	0.82	250	450	1	1	none
918911			1.6	250	550	1	1	none
918911			1.8	250	650	1	1	none
918911			3	250	600	15	1	none

TRANSIENT REFLECTIVITY

Transient Reflectivity (TR) can be a sensitive probe of the surface of a semiconductor, but the reflection coefficient involves the complex dielectric function (which is determined by the spectral characteristics of the carrier population over the entire spectrum). Ordinarily, fs white light is used as the probe in pump probe measurements in order to map the response as a function of wavelength. In this measurement both the pump and probe are 620 nm pulses from a CPM laser. This allowed measurements to be made at the same wavelength as the photoconductive excitation used in electro-optic and THz spectroscopy measurements.

For the measurements shown in Fig. 1, the samples received a Rapid Thermal Anneal (RTA) (if used). The data is presented as acquired (no normalization). Qualitatively similar data for intrinsic GaAs as a function of wavelength has been reported [4]. We see that for anneals $< 450^\circ\text{C}$ there is no difference in the TR response (The unannealed sample may have different scaling). Three samples were chosen to be fabricated into photoconductive switches: anneals at 450, 550, and 650°C . These represent three different qualitative TR responses: unannealed-like, intermediate, and semi-insulating-like behavior. We see from the electro-optic data of Fig. 2(b) that for these samples, the fastest response corresponds to the lowest temperature anneal, despite the fact that the smallest (and fastest) response in TR corresponds to a higher 550°C anneal.

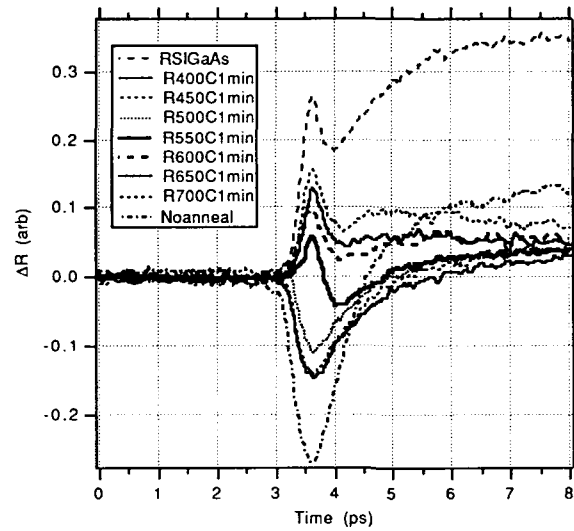


Figure 1. Transient reflectivity 620 nm (pump and probe) result. Anneals are 1 min.

ELECTRO-OPTIC PULSEWIDTH MEASUREMENT

Electrical characterization was performed using electro-optic sampling [5] with sub-millivolt sensitivity [6] based on a Colliding Pulse Mode locked (CPM) laser.

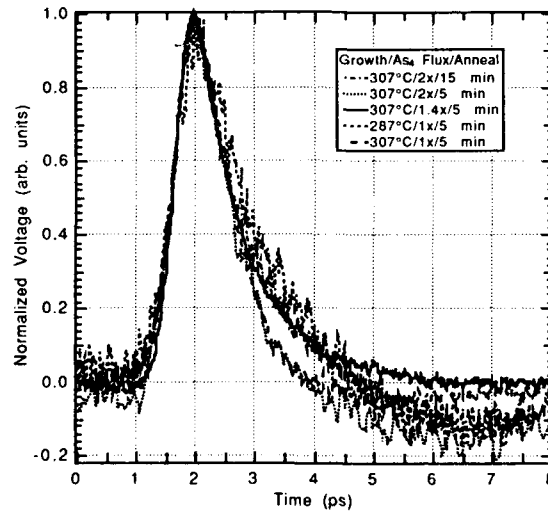


Figure 2(a). Electro-optic sampling data. For As₄ fluxes varying by a factor of two there is essentially no change in pulsewidth.

Figures 2(a) and 2(b) show the results for some of the growth conditions listed in Table I. Coplanar strip transmission lines were fabricated with $5\ \mu\text{m}$ line widths and spacing. Electrodes were $0.2\ \mu\text{m}$ thick evaporated Au. The data are acquired using a large ($>1\ \text{mm}$ wide \times $500\ \mu\text{m}$ thick) LiTaO_3 crystal (in a reflection mode geometry at $620\ \text{nm}$) to delay electrical reflections until later times (i.e. times later than the temporal window of interest). All curves have been normalized to facilitate comparisons of the pulsewidth. In addition, the individual time axes have been adjusted to a common origin. In addition to the data shown in Fig. 2 other samples were characterized, the results summarized in Table I. Note that the sample doped to $10^{17}/\text{cc}$ had the same pulsewidth as the samples grown without doping. The 450°C sample had a small ($\sim 100\ \mu\text{A}$) dark current.

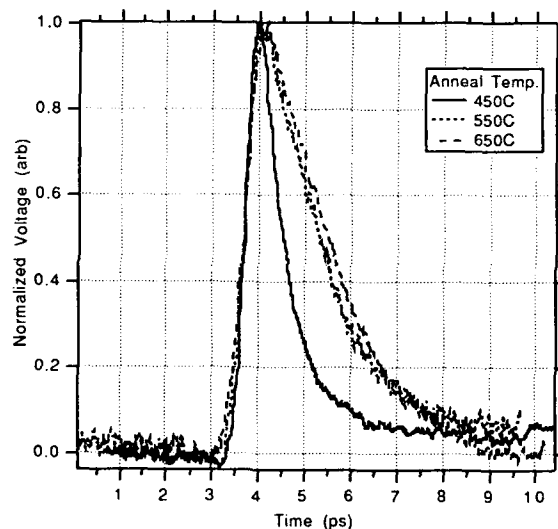


Figure 2(b). Electro-optic sampling data. For RTAs varying by only 50°C , there is a decrease of 50% in pulsewidth (from ~ 1.8 to $0.8\ \text{ps}$).

PULSED TERAHERTZ SPECTROSCOPY

Pulses of microwave [7] and millimeter wave radiation [8-11] can be generated using visible short pulse lasers. Detecting this radiation has so far been limited by the sampling gate used in the receiving antenna. Using a far-infrared interferometer, RF pulses as short as $160\ \text{fs}$ FWHM have been detected [12]. Using a $10\ \text{Hz}$ amplified CPM laser, optical pulses $\sim 0.5\ \text{mJ}$ are produced. These pulses are used to illuminate an $\text{InP } \langle 111 \rangle$ wafer which produces an RF burst at the specular reflected angle. The RF can be focussed using off axis parabolic mirrors to a spot size of about $0.5\ \text{cm}$ corresponding to the lowest frequencies in the radiated spectrum.

Freestanding wire-grid polarizers and Au coated mirrors are used to form the interferometer. Detection is accomplished using a commercial liquid helium cooled bolometer with a composite Si-on-diamond element. This technique has been used to study carrier dynamics in intrinsic GaAs with subpicosecond resolution [13]. Figure 3(a) shows the $620\ \text{nm}$ pump, far-infrared probe measurements corresponding to the electro-optic results in Fig. 2. The data show little variation for change in As_4 flux of a factor of two, as is the case for the data of Fig. 2(a). In addition, a long lived tail is evident which does not appear in the electro-optic measurement. This may be evidence of carrier localization, as the electro-optic

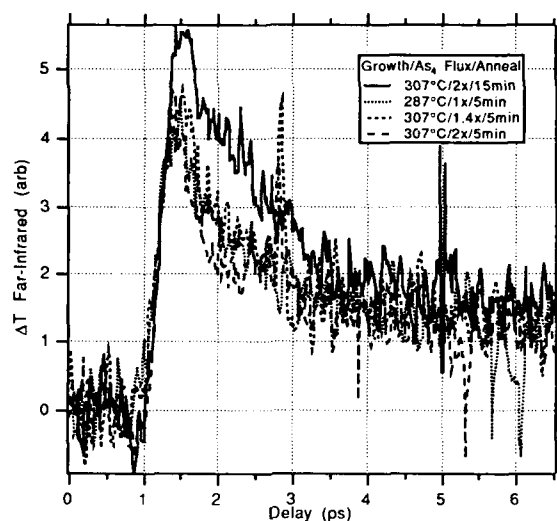


Figure 3(a). Pump (620 nm) and THz probe of several LT GaAs wafers grown with different As_4 fluxes. Legend refers to flux times flux for normal growth conditions.

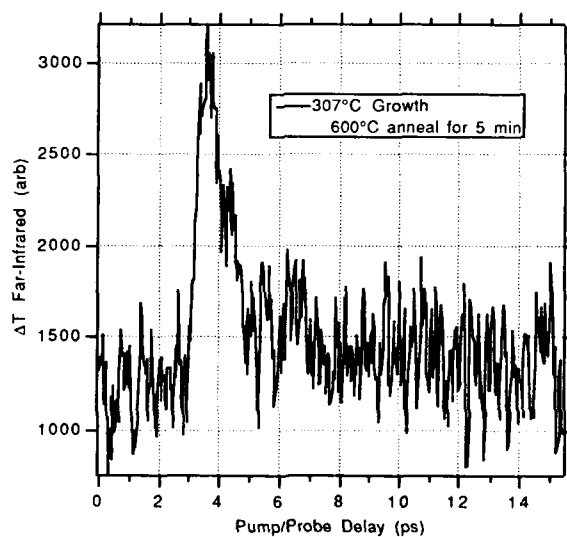


Figure 3(b). Pump (620 nm) and THz probe of an LT GaAs wafer for a longer time window. The THz and electro-optic measurements are both ~ 1.1 ps FWHM.

measurement is sensitive only to mobile carriers while THz spectroscopy measures the total carrier population. However, the sample of Fig. 3(b). shows little evidence of such a tail, and there is good agreement between the electro-optic and THz measurements, both about 1.1 ps FWHM.

TRANSMISSION ELECTRON MICROSCOPY

Samples for cross-section transmission electron microscopy (TEM) were prepared by mechanically polishing to a thickness of $\sim 80\mu\text{m}$ and then ion milling to perforation at 3-5kV with either argon or iodine at either room temperature or liquid nitrogen temperature. No specimen preparation artifacts were observed. TEM was performed principally at either 120 or 200kV in order to minimize electron beam damage. Measurements of As precipitate density and volume fraction of precipitates listed in Table I were found using TEM. In addition, an in situ anneal was performed to investigate the pulsewidth dependence on anneal temperature. Measurements on wafers with no previous anneal history showed that precipitation occurred at a *particular* temperature around 500 °C. Exact measurement of the sample temperature was not possible due to the geometry of the sample. Slightly longer or hotter anneals did not significantly alter the density of precipitates.

CONCLUSION

In this paper we have presented several key observations about the nature of picosecond photoconductivity in LT GaAs. First, the annealing history of a given LT GaAs switch in large part determines its photoresponse. Second, we have presented evidence for a thermal activation temperature for short pulse photoconductivity. This was measured directly, using electro-optic sampling, and indirectly using transient reflectivity, pulsed terahertz spectroscopy and transmission electron microscopy. We have also found no change in electrical pulsewidth corresponding to a range of more than an order of magnitude in As precipitate density or for a doping level of $10^{17}/\text{cm}^3$.

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A NEW STRUCTURE FOR A SUPERCONDUCTING FIELD EFFECT TRANSISTOR

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ABSTRACT

A new structure is proposed and described which can solve the most severe drawbacks of current architectures for Josephson FETs. Its advantages are discussed, and several realizations are suggested.

INTRODUCTION

Logic operation based on the Josephson effect is very attractive because of its high speed and low dissipation. However, it is difficult to build all logic functions using only Josephson Junctions (JJ). For that reason, there have been numerous attempts to make transistors that utilize superconductivity in one way or another so that they can be interfaced with JJs and bring the essential three terminal functions to JJ circuits. Of the many proposals (see e.g. [1][2] for a review of the more classic ones, and [3] for an introduction to the single flux quantum logic family) perhaps the most straightforward is the JOFET (Josephson Field Effect Transistor) [4].

In this paper, we first introduce the JOFET and recall oft quoted arguments [5] which lead to the conclusion that it has little future as a useful device. Secondly, we propose a sister design: the Superconducting PERcolating Field Effect Transistor (SUPERFET), that has the potential of becoming a useful device, and we discuss several possible realizations of the SUPERFET. All the discussion could be translated advantageously in terms of high temperature superconductors but we restrict ourselves to conventional ones.

THE JOFET

A JOFET has essentially the same design as a normal FET, the only difference being that the source and drain are made of a superconductor (lead and niobium are frequent choices). A supercurrent can then flow between source and drain (see Fig. 1.a) through the semiconductor because

of the proximity effect. Cooper pairs leak from the superconductor into the adjacent semiconductor where they have a finite lifetime $\tau = \hbar/2\pi k_B T$ [6]. These Cooper pairs travel in the semiconductor at the velocity v of quasi-particle excitations. This velocity depends on the particular semiconductor used. One associates with the lifetime and the velocity, a characteristic length ξ for the exponential decay of the number of Cooper pairs, into the semiconductor and away from the superconducting interface. One usually discerns two cases. In the clean limit, the Cooper pairs die before they collide, and the characteristic length is given by $\xi_C = v\tau$. In the dirty limit, the Cooper pairs experience many collisions before they collapse, and the length is $\xi_D = \sqrt{D\tau}$ where D is the diffusion coefficient. The transistor effect is obtained by imposing a gate voltage V_G which decreases or increases the number of electrons in the channel and thereby acts upon the velocity v , and on the decay length $\xi(V_G)$ [7].

The maximum supercurrent I_c which can flow from source to drain is given by

$$I_c = A \exp(-L/\xi(V_g)), \quad (1)$$

where L is the source to drain distance, as shown on Fig. 1, and A is a prefactor which represents essentially the boundary conditions between the semiconductor and the superconductor. In particular, A depends exponen-

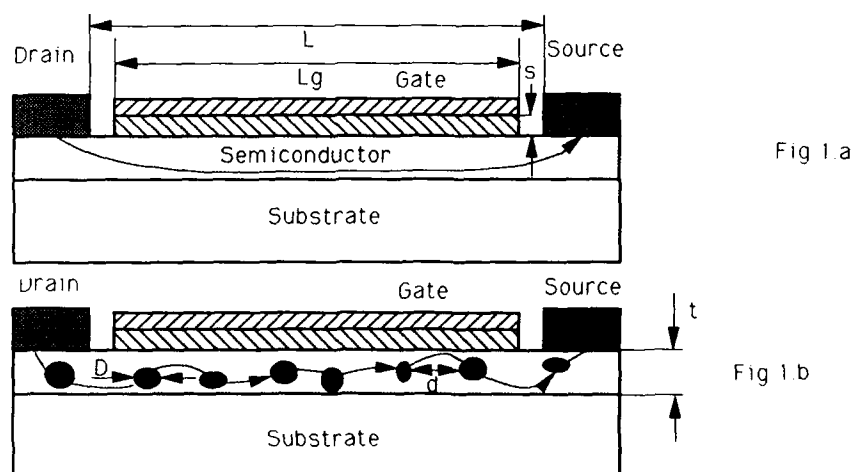


Fig. 1: 1.a JOFET the metallic gate is on an insulator, source and drain are made of a superconductor, Cooper pairs must travel the distance L . 1.b In the SUPERFET the Cooper pairs hop between neighbouring (average distance d) superconducting precipitates.

tially on the barrier height. This expression for the supercurrent imposes obvious constraints on the design of a JOFET : the source to drain distance should be comparable to ξ , and the Schottky barrier at the super/semiconductor interface should be as small as possible, otherwise the supercurrent will be reduced to nothing.

Let us turn to the characteristics of a JOFET[5]. To a first approximation, it looks exactly like a conventional FET (see the characteristic on Fig. 2). In order to see the difference, one must zoom in on the low voltage region of Fig. 2, as shown in the inset. There, one notices a supercurrent which depends on the applied gate voltage. It is easily seen that the interesting mode of operation (i.e. where it is different from a conventional FET) is confined to a few times Δ/e (where Δ is the superconducting gap), that is to say a few millivolts. By contrast, the gate voltages required to modulate the supercurrent are of the same order as for a conventional FET, i.e. at least 100mV. Voltage gain seems to be out of reach for these devices, because of two irreconcilable goals: the need to increase ξ in order to reach lithographically manageable dimensions, and the need to lower the doping in order to have small control voltages.

JOFETS will continue to be essential to confront the theoretical predictions which have been, so far, well tested only in metals. The dependence of ξ on temperature is predicted to be B/T in the clean limit, and B'/\sqrt{T} in the dirty limit. Both regimes have been convincingly observed with the

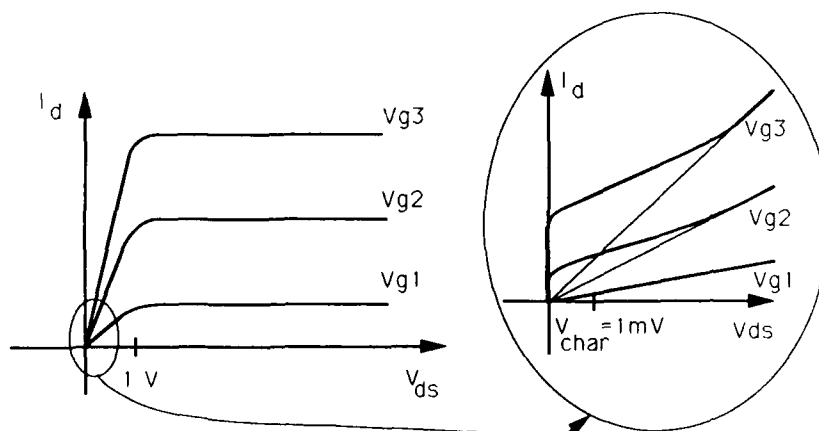


Fig. 2: Characteristics of a JOFET, I_d is the drain current, V_g is the gate voltage. It differs from a FET only at low voltages.

right constant B or B' in the case where the non superconducting material is a normal metal (see e.g. the beautiful experiment of Mota et al. [8]). However, the situation is less clear in the case of semiconducting links. The dependence of ξ on the number of carriers n has been predicted to be $\xi \propto n^{1/3}$, both in the clean and in the dirty limit [9], in the case of a degenerate semiconductor. These predictions lack strong experimental confirmation and need more investigation.

THE SUPERFET

The main problems which plague the JOFET and essentially render it hopeless as a useful device can be cured simultaneously if one considers the following new structure illustrated in figure 1.b. Superconducting precipitates immersed in a thin film semiconducting matrix can act as the channel of a FET bringing about the following improvements. A) The distance between the precipitates is now a material parameter and can, hopefully, be varied at the growth stage. It can therefore be made much smaller than lithographically defined structures. B) As a consequence, the decay lengths in the semiconductor can be much smaller. This, in turn, opens the way for comparatively lightly doped semiconductors to be used and reduces the required gate voltages. C) In this configuration, there are N junctions in series and the characteristic voltage is multiplied by N . *Voltage gain can thus, in principle, be achieved.*

In order to illustrate our proposal, let us discuss the relevant dimensions and material parameters required when InAs is used as the semiconducting matrix.

The superconducting precipitates have a mean diameter D which should be as small as possible so as to accommodate many junctions in series over the gate length L_g . The lower limit on the diameter under which small particles cannot become superconducting has been evaluated [10][11]. For lead, a critical diameter of 22\AA has been calculated for isolated particles[11]. In the case of lead particles in contact with a semiconducting matrix, the proximity effect weakens superconductivity and therefore, increases the minimum diameter. However, the lowering of the critical temperature is weaker for a semiconductor than for a normal metal and depends critically upon the boundary conditions. It is reasonable to think that lead particles with diameters of the order of 200\AA will be superconducting robustly enough to form the channel of our SUPERFET.

The distances between particles should also be as small as possible without shorting the channel. In order to give an estimate, one can choose $d = 500\text{\AA}$. Ideally, the particles would be nucleated at the interface with the substrate and the thickness of the channel t would be of the same order as the inter-particle distances $t \approx 400\text{\AA}$.

With those numbers, and a gate length of $1.4\mu\text{m}$ one has twenty junctions in series and the response voltage can become $V_{\text{char}} \gtrsim 20\text{mV}$. Now, suppose the semiconductor is n type InAs with effective mass $m^* = 0.023m_e$, and doping level $n = 10^{16}\text{cm}^{-3}$, one gets a clean limit coherence length of

$$\xi_C = (\hbar^2/2\pi m^* kT)(3\pi^2 n)^{1/3} \approx 1000\text{\AA}, \quad (2)$$

with n the density of free electrons and $T = 4\text{K}$. If the material is in the dirty limit, the coherence length would be smaller and of order 150\AA which is still acceptable. With such a comparatively low doped channel, the gate voltage required to deplete the SUPERFET is reduced accordingly. The depletion length W for a gate voltage V_g is given, in the case of a metal insulator FET, by,

$$W(V_g) = s \frac{\epsilon_{sc}}{\epsilon_{ox}} \left[\sqrt{1 - \frac{2V_g \epsilon_{ox}^2}{s^2 e n \epsilon_{sc}}} - 1 \right], \quad (3)$$

where s is the thickness of the insulator, e the charge of an electron, ϵ_{sc} and ϵ_{ox} are the dielectric constants of the semiconductor and the insulator respectively. For $V_g = -40\text{mV}$, $s = 100\text{\AA}$, $\epsilon_{sc} = 14.6$, and $\epsilon_{ox} = 3$, one gets $W \approx 450\text{\AA}$, enough to deplete the channel. The ratio $V_{\text{char}}/V_g \gtrsim 1/2$ is closer to 1. In order to really achieve voltage gain, one should use a lower doping for the semiconductor. However, this would lead to the breakdown of the simple picture that we have used of the semiconductor as a metal with very few electrons. This low doping regime is probably of great experimental interest but has had very little attention so far because of the difficulties inherent with its observation.

We would now like to briefly discuss two materials among several that may be useful for the SUPERFET.

A) *Lead chalcogenides*. The superconductivity of lead salts (PbS) when it is over stoichiometric in Pb was observed as far back as 1947 [12]. More recently, Indium doped $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$ films with lead precipitates have shown an enhancement of the superconducting temperature as a function of photoemission of carriers [13]. It was postulated that lead precipitates in the form of small spherical inclusions [13]. We have carried out a Transmis-

sion Electron Microscopy study of superconducting PbSe [14][15][16], and we have observed well crystallized spherical lead precipitates which do not disturb the crystallinity of the host PbSe matrix.

Work is in progress on this material which is interesting in particular because of its low effective mass ($m^* = 0.045$) and of the fact that lead precipitates naturally.

B) *LT-GaAs*. Low Temperature Grown GaAs has recently been shown to have superconducting inclusions under 10K [17]. However, so far, no experiments have demonstrated the zero resistance behavior expected when the proximity effect is strong enough.

If LT-GaAs exhibits the proximity effect somewhat as lead salts do, it will become a favorite material for the SUPERFET, because of its industrial importance and because of the favorable material parameters such as a small effective mass for electrons ($m^* = 0.067$).

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PART IV

In-Based and Other Compound
Semiconductor Materials Grown
at Low Temperatures

THE USE OF LCW TEMPERATURE AlInAs AND GaInAs LATTICE MATCHED TO InP IN THE FABRICATION OF HBTs AND HEMTs

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ABSTRACT

AlInAs and GaInAs lattice matched to InP and grown by MBE over a temperature range of 200 to 350°C (normal growth temperature of 500°C) has been used to enhance the device performance of inverted (where the donor layer lies below the channel) High Electron Mobility Transistors (HEMTs) and Heterojunction Bipolar Transistors (HBTs), respectively. We will show that an AlInAs spacer grown over a temperature range of 300 to 350°C and inserted between the AlInAs donor layer and GaInAs channel significantly reduces Si movement from the donor layer into the channel. This produces an inverted HEMT with a channel charge of $3.0 \times 10^{12} \text{ cm}^{-2}$ and mobility of $9131 \text{ cm}^2/\text{V-s}$, as compared to the same HEMT with a spacer grown at 500 °C resulting in a channel charge of $2.3 \times 10^{12} \text{ cm}^{-2}$ and mobility of $4655 \text{ cm}^2/\text{V-s}$. We will also show that a GaInAs spacer grown over a temperature range of 300 to 350°C and inserted between the AlInAs emitter and GaInAs base of an npn HBT significantly reduces Be movement from the base into the emitter, thereby allowing higher Be base dopings (up to $1 \times 10^{20} \text{ cm}^{-3}$) confined to 500 Å base widths, resulting in an AlInAs/GaInAs HBT with an f_{max} of 73 GHz and f_t of 110 GHz.

INTRODUCTION

$\text{Al}_{0.48}\text{In}_{0.52}\text{As}$ and $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ lattice matched to InP are extremely useful for high-speed electronic and optical devices [1-2]. Device applications often require high resistivity, low lifetime material to act as buffers for electrical isolation and reduction of backgating and sidegating [3-6]. It has been demonstrated that these characteristics can be obtained using lattice matched materials grown at temperatures substantially below those of normal growth conditions in which excess As in quantities of 1-2% are present. This growth regime is often referred to as Low Temperature (LT) growth [3-6]. There is, however, an intermediate growth regime between that of normal growth (500 to 600°C) and LT growth (below 200°C) in which there is little to no excess As, but in which the movement of dopant atoms has been significantly reduced, compared with material grown at normal temperature [7-11]. We have utilized this intermediate growth regime to produce AlInAs and GaInAs that inhibits the movement of Si and Be, but is not so heavily defected or the lifetime so degraded that it becomes unsuitable for use in the active regions of HEMTs and HBTs.

EXPERIMENTAL

The epitaxial layers were grown in Perkin Elmer PHI-430 and Riber 2300 MBE systems. The substrate temperature was referenced to the (2×4) to (4×2) surface transition as determined by Reflected High Energy Electron Diffraction (RHEED) patterns that occurs upon heating the InP substrate in an As_4 beam before growth is initiated. For these experiments, using an As_4 beam equivalent pressure of 8 to 12×10^{-6} Torr, we assume that this transition occurs at 540°C and reference all other temperatures to it. Growth rates of both AlInAs and GaInAs were 100 Å/min with lattice mismatch, as determined by x-ray rocking curves, held to within 1% of lattice matched conditions. Secondary Ion Mass Spectroscopy (SIMS) measurements were performed at Charles Evans and Associates. During LT growth and normal growth, the As_4 overpressure was maintained during all substrate temperature ramps between low temperature and normal temperature growths - there was no interruption of the As_4 overpressure. Specific details of normal temperature

and low temperature AlInAs/GaInAs growth [6-12], and device and circuit fabrication are given elsewhere [13-15].

RESULTS

AlInAs

SIMS analysis was performed on a test structure that consisted of a 2500 Å AlInAs buffer layer (grown at normal temperature) followed by five periods of a GaInAs/AlInAs inverted modulation doped structure. This structure consisted of 450 Å of AlInAs (grown at normal temperatures), a silicon delta-doped layer of either 1.5×10^{12} or $3.0 \times 10^{12} \text{ cm}^{-2}$, a 50 Å AlInAs spacer grown at either 500, 425, 350, or 275°C, and finally a 500 Å GaInAs layer. The 275°C layer was grown twice, once at the beginning of growth and once at the end of growth to determine resolution changes with depth of the layer, as well as possible diffusion effects that may occur for the spikes grown earlier in the run and subsequently held at an elevated substrate temperature until the completion of the run. Figure 1 shows the results of SIMS analysis on this sample (for two different delta doping levels), in which the rate of decay (the distance required for the doping level to decrease by one order of magnitude) of the Si spike through the 50 Å LT AlInAs spacer and into the 500 Å GaInAs channel is measured as a function of the LT AlInAs spacer growth temperature.

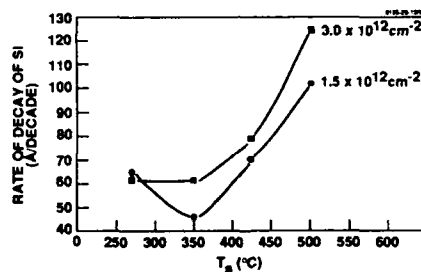


Figure 1. Rate of decay of silicon versus substrate growth temperature through a 50 Å LT AlInAs spacer.

For both doping levels, a significant increase in the slope (approximately a factor of 2) occurs when the growth temperature of the spacer layer is reduced from 500 to 350°C. No reduction in the rate of decay is observed by further lowering the growth temperature to 275°C. Therefore, the optimum growth temperature of the LT AlInAs spacer in order to inhibit the movement of Si from the AlInAs donor layer into the GaInAs channel of an inverted HEMT is in the range of 300 to 350°C.

GaInAs

Four Be planar doped spikes were grown in GaInAs, whose concentrations varied from 1.0 to 0.017 monolayers and were each separated by 2500 Å. The GaInAs was grown at a substrate temperatures of 445, 370, 315 and 225°C. The full width at half maximum (FWHM) of each Be spike was measured by SIMS. Figure 2 shows the L (normalized), which is defined as the FWHM of a given monolayer coverage normalized to the FWHM grown at 445°C, as a function of the growth temperature.

For GaInAs growth below 350°C, the FWHM decreases rapidly by a factor of approximately 3 as compared to those grown under normal conditions. Two interesting features of Figure 2

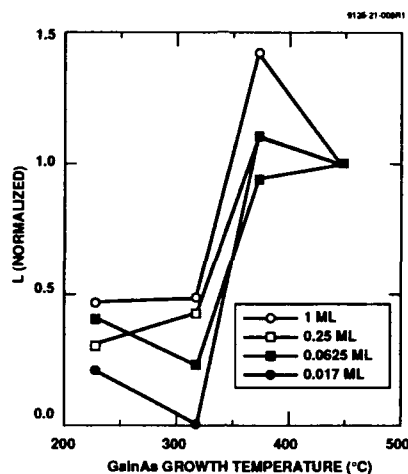


Figure 2. L(normalized) of Be planar doped spikes in GaInAs at a given Be monolayer coverage versus growth temperature.

are that there is no significant decrease in the FWHM for growth below 350°C, and that the growth in the 400°C range appears to actually enhance the Be diffusion as compared to growth at 445°C. These results indicate that the optimum growth for LT GaInAs in order to inhibit Be diffusion should take place at 300°C, since any lower temperature does not decrease the Be FWHM.

Inverted HEMTs

Figure 3 is a schematic of a typical inverted GaInAs/AlInAs HEMT. For this experiment the channel thickness was 200 Å and the LT AlInAs spacer, grown at 300°C in order to inhibit Si movement from the delta doped layer into the channel, was varied from 30 to 100 Å. The designed 2DEG charge was varied from 1.5 to 3.0×10¹² cm⁻².

Figure 4 is a plot of the 300 K electron mobility for the inverted HEMT shown in Figure 3 with different AlInAs spacer thicknesses and spacer growth temperatures of either 500 or 300°C. The mobility obtained using the low temperature spacer is comparable to that which would be obtained in a normal structure (the donor layer above the channel) for a similar 2DEG density.

70Å	Ga _{0.47} In _{0.53} As	CONTACT	
200Å	Al _{0.48} In _{0.52} As	BARRIER	
200Å	Ga _{0.47} In _{0.53} As	CHANNEL	
60Å	Al _{0.48} In _{0.52} As	SPACER	SI PLANE,
2500Å	Al _{0.48} In _{0.52} As	BUFFER	δ-DOPED
InP SUBSTRATE			

Figure 3. Schematic of inverted HEMT.

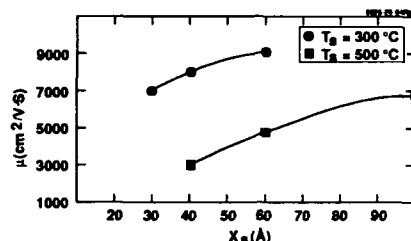


Figure 4. Electron mobility versus spacer layer thickness for 500 and 300°C spacer layer growth temperature.

Significant degradation of the mobility is seen to occur for the samples grown in which the AlInAs was grown at normal temperature. It should also be noted that the thicker the spacer the less the degradation, giving further indication that the degradation mechanism is due to the movement of Si through the spacer and into the channel.

Figure 5 shows the dc I-V characteristics of an inverted AlInAs/GaInAs HEMT that uses a LT AlInAs spacer. The sheet charge and mobility of this structure were $3 \times 10^{12} \text{ cm}^{-2}$ and $9100 \text{ cm}^2/\text{V-s}$, respectively. Devices with $0.2 \mu\text{m}$ gates were fabricated and exhibited transconductances of 800 mS/mm , f_t 's of 100 GHz , and f_{max} 's of 170 GHz . The dc output conductance of 28 mS/mm is much better than that typically obtained in a normal GaInAs/AlInAs HEMT structure, and no kink effect was observed in the I-V characteristics.

HBT

Figure 6 shows our AlInAs/GaInAs HBT, in which two low temperature GaInAs spacers grown at 300°C are placed at the emitter-base interface. These two spacers are intended to impede the movement of Be from the base to the emitter. Five different LT GaInAs spacer configurations, T1 through T5, were grown as shown in Table I, consisting of both doped and undoped LT GaInAs. The Be level in the base has been targeted at $1 \times 10^{20} \text{ cm}^{-3}$ based on the maximum doping that can be confined by LT GaInAs as determined by the planar doped experiments described above.

Figure 7 shows the resultant SIMS profiles for the five cases shown in Table I, in which the Si, Be and Al (intensity uncalibrated) are being profiled. Optimum HBT performance[15] occurs for the Be and Si electrical junction being coincident at the AlInAs/GaInAs heterojunction. In Figure 7, an indication that Be has diffused into the AlInAs is denoted by the hump in the Be

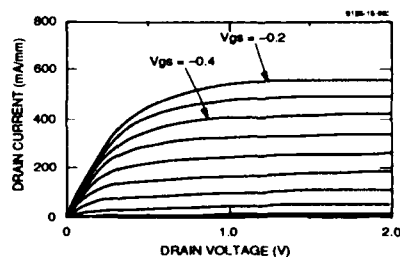


Figure 5. DC I-V characteristics of inverted HEMT.

GaInAs	CONTACT	$n \approx 1 \times 10^{19}$	1000 Å
AlInAs	EMITTER	$n \approx 1 \times 10^{19}$	700 Å
AlInAs	EMITTER	$n \approx 8 \times 10^{17}$	1500 Å
Low Temp. GaInAs 300°C	SPACER 1		
Low Temp. GaInAs 300°C	SPACER 2		
GaInAs	BASE	$p \approx 1 \times 10^{20}$	500 Å
GaInAs	COLLECTOR	$n \approx 1 \times 10^{18}$	3000 Å
GaInAs	SUBCOLLECTOR	$n \approx 1 \times 10^{19}$	7000 Å
GaInAs	BUFFER	undoped	100 Å

Figure 6. AlInAs/GaInAs HBT with two LT GaInAs emitter-base spacers.

Table I. Spacer thicknesses (Å) and doping levels (cm^{-3}) for LT GaInAs spacers (grown at 300°C) and bases for HBT shown in Figure 6

Sample	Spacer 1	Spacer 2	Base
T1	50Å undoped	0Å undoped	500Å 1×10^{20}
T2	0Å undoped	150Å 2×10^{18}	500Å 1×10^{20}
T3	0Å undoped	75Å 2×10^{18}	500Å 1×10^{20}
T4	0Å undoped	0Å undoped	500Å 1×10^{20}
T5	0Å undoped	150Å 1×10^{20}	350Å 1×10^{20}

profile when it crosses into the AlInAs, because of the increased secondary ion yield of AlInAs as compared to GaInAs. This hump is therefore an excellent indication of Be penetration. The control sample, case T4 (that without any spacer), shows Be penetration of almost 1000 Å into the emitter, while a minimum of 75 Å of LT GaInAs doped at $2 \times 10^{18} \text{ cm}^{-3}$ (case T3) will hold the Be in place. To enhance reliability, we chose case T2 as the standard npn HBT structure employing 150 Å of LT GaInAs grown at 300°C and doped at $2 \times 10^{18} \text{ cm}^{-3}$. HBTs fabricated using the T2 profile have obtained current gains of 23 with an f_{max} of 73 GHz and f_t of 110 GHz. Higher gains may be obtained by lowering the base doping and trading lower f_{max} for higher gains.

CONCLUSIONS

We have shown that there is a significant reduction in the movement of Si in AlInAs and Be in GaInAs when the material is grown in the temperature range of 300 to 350°C. This LT material was then used to enhance the device performance of both inverted HEMTs and npn HBTs.

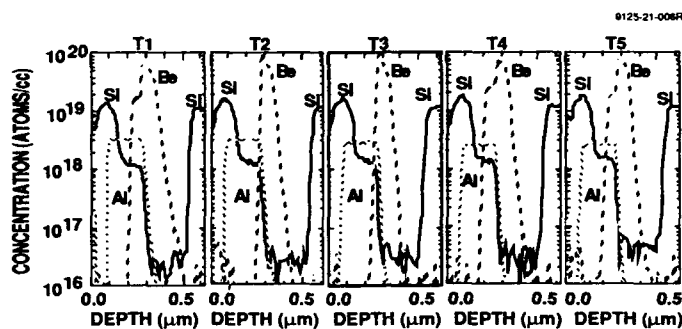


Figure 7. SIMS profiles of the five spacer configurations listed in Table I showing Si, Be and Al (uncalibrated intensity).

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INP LAYERS GROWN BY MOLECULAR BEAM EPITAXY AT LOW SUBSTRATE TEMPERATURE

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ABSTRACT

InP layers were grown on semi-insulating InP wafer by molecular beam epitaxy (MBE) at low substrate temperatures ($< 200^{\circ}\text{C}$), using solid phosphorus source. We use x-ray diffraction, double crystal x-ray rocking curve, Auger electron spectroscopy, and temperature-dependent Van der Pauw and Hall effect measurements to characterize the as-grown and annealed InP layers. It is found that the InP layer is in poly-crystal state with excess P over 7 at%. The layers became single crystal after annealing above 400°C . The resistivity of the InP layer decreased from $60\ \Omega\text{cm}$ for an as-grown sample to $0.82\ \Omega\text{cm}$ after 400°C RTA annealing. The different role of excess P as compared to the role played by excess As in LT-GaAs is discussed based on the P properties.

INTRODUCTION

InP is an important compound semiconductor material for high speed electronic and optoelectronic devices. The sidegating and backgating problems associated with InP based devices require a substrate with improved electrical properties. Recently, GaAs grown by molecular beam epitaxy (MBE) at low substrate temperature (LT-GaAs) has been shown to be a promising material [1]. The use of LT-GaAs as a buffer layer led to a great reduction of sidegating and backgating, and an increase in breakdown voltage in FETs [1, 2]. Successful growth of other As-based compounds such as AlGaAs and AlInAs have been reported, showing properties similar to LT-GaAs [3, 4]. Typical characteristics of these LT materials are (1) large amount of excess As (up to 1~2at%), (2) high density of defects such as As precipitates and As_{Ga} antisite defects, and (3) a relatively high crystalline quality. Further extension of low substrate temperature growth to InP would be of great interest. Norris [5] had reported MBE growth of InP at various substrate temperatures. But he did not study the stoichiometry and annealing behavior of InP layer grown at low substrate temperatures ($< 300^{\circ}\text{C}$). In this paper, we report the growth and materials characteristics of LT-InP. The growth is performed at different substrate temperatures and P over-pressures. Electrical and structural properties, and annealing behavior of these LT-InP layer are reported. Implications of our results are also discussed.

INP GROWTH

The Riber 32P MBE system with a valved, solid phosphorus source which has

been described previously [6] is used to grow the InP layer. Red phosphorus is used as the phosphorus beam source. The phosphorus source temperature was kept at 350°C with the temperature of the cracker zone kept at 1000°C. The P₂ beam flux was controlled by varying its equivalent vapor pressure. Fe-doped semi-insulating (100) InP wafers were used as substrates. The InP substrate was baked at 250°C for 1 hour before growth started. Two series of InP layers were grown. In the first series of growths, the P₂ flux was kept constant with a vapor pressure at 8×10^{-5} Torr which is the same as that used in normal substrate temperature growth. The substrate temperature was varied from 300°C to 100°C. In the second series of growths, the substrate temperature was kept constant at 200°C and the P₂ flux was reduced to 1/2 and 1/4 of the normal P₂ flux, respectively. All layers are grown at a rate of 1 $\mu\text{m/h}$. The thickness of each layer and other growth parameters are listed in Table 1.

STRUCTURAL AND ELECTRICAL PROPERTIES

InP layers were examined by Auger electron spectroscopy (AES) to determine the layer stoichiometry. The sample surfaces were cleaned by sputtering with 5keV Ar ion for 30sec before AES measurements. The results are summarized in Table 1. The InP layers grown at 200°C and 100°C with normal P₂ flux have 7at% and 11at% excess P respectively. The InP layer grown at 200°C with 1/4 normal P₂ flux shows phosphorus deficiency. All InP layers had mirror-like and featureless surfaces except for the sample grown with 1/4 normal P₂ flux. The surface of this sample became granular. The crystalline quality of the layers were further studied by x-ray diffraction. The x-ray rocking curve with FeK _{α 1} of the (400) plane showed only one diffraction peak on all the as-grown samples. The InP layer grown at 300°C had a good crystalline quality indicated by its values of reflecting power and FWHM as compared to that of a single crystal InP wafer. However, the reflecting power was reduced by more than 70% as the growth temperature decreased to 200°C or 100°C. X-ray diffraction measurements taken on LT-InP

Table 1. Structural and Electrical Properties of LT-InP

Sample #	Growth Temp. Ts	P2 Vapor Pressure (Torr)	InP Layer Thickness	Stoichiometry	Crystallinity	Maximum Resistivity (Ωcm)	Mobility (cm^2/Vs)	
							As-grow	400 C Annealing
^a 539	300 C	8×10^{-5}	5 μm		single crystal			
560	200 C	8×10^{-5}	5 μm	7 at% excess P	poly-crystal	24.6	320	993
561	100 C	8×10^{-5}	5 μm	11 at% excess P	poly-crystal	60.0	337	1014
592	200 C	4×10^{-5}	2.5 μm		poly-crystal	3.96	212	326
591	200 C	2×10^{-5}	2.5 μm	P deficient	poly-crystal	1.10	51	307

a. There was an accumulation of impurity on the sample surface due to the incident. It is difficult to recover the sample for electrical measurement. The structure characterization data is reliable.

indicated that the LT-InP layers are not single crystal as evidenced by the appearance of a broad (111) diffraction peak as shown in Fig.1. The Raman spectroscopy measurement of LT-InP layers confirmed the x-ray diffraction result. Thus, it is believed that these LT-InP layers are in a poly-crystalline state. The greatly reduced (400) diffraction peak in the x-ray rocking curve may come from the substrate and/or the single crystal portion of the LT-InP layer. Our results are similar to what Norris had observed[5] but the transition temperature from single crystal to poly-crystal is lower in Norris' case ($< 150^{\circ}\text{C}$). The different layer thickness (1 μm thick layer for Norris samples) and other growth parameters may have attributed to this difference. It has been reported that there is a thickness limit ($\sim 2\mu\text{m}$) for single crystal epitaxial LT-GaAs layers [7, 8]. It was speculated that the $\text{P}_2 + \text{P}_2 \rightarrow \text{P}_4$ reaction may be responsible for the large amount lattice disorder and cause a (111) oriented island growth [5].

Resistivity and Hall mobility of as-grown LT-InP layers were determined by the Van der Pauw and Hall effect measurements. The resistivity increased with decreasing the growth temperature and decreased with the reduction of P_2 flux. The room temperature mobility values are in the range of 200 ~ 500 cm^2/Vs and increase with measurement temperature from 80k to 400k. The InP layer grown with 1/4 P_2 flux has a very small mobility which is invariant with measurement temperature.

ANNEALING STUDY OF LT-InP

All LT-InP layers were subjected to an isochronal RTA annealing at temperatures ranging from 200°C to 600°C for 15 s. X-ray double crystal rocking curve shows that, for the InP layers grown at 200°C and 100°C with normal P_2 flux, after a 200°C or 250°C RTA annealing, a satellite peak appears on the left side of substrate (400) diffraction peak as shown in Fig.2. With further increase of annealing temperature, the satellite peak moves and merges with the original (400) diffraction peak. However, for the samples grown with 1/2 and 1/4 P_2 flux, there is no satellite peak in the x-ray rocking curves after the annealing. The X-ray reflecting powers of all samples increased with the annealing but

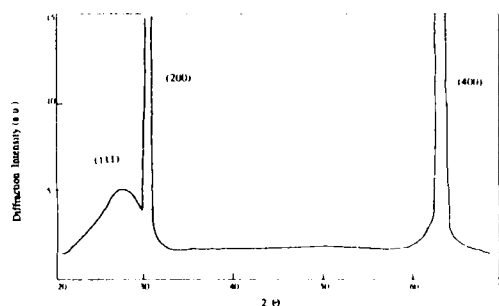


Fig.1 X-ray diffraction curve of the sample grown at 200°C with normal P flux.

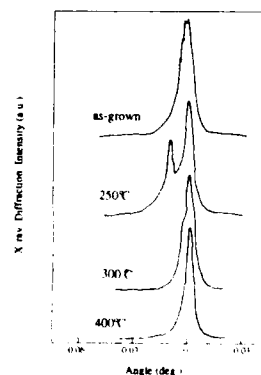


Fig.2 X-ray rocking curves of the sample grown at 200°C with normal P flux and annealed by RTA for 15s.

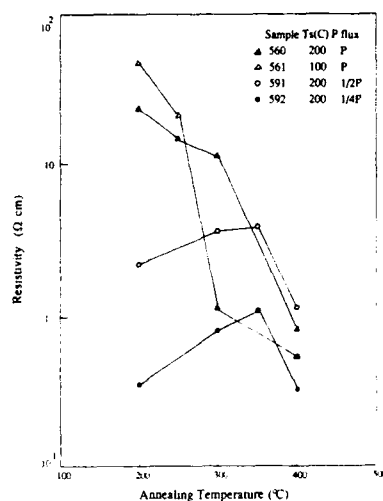


Fig.3 Resistivity vs annealing temperature of LT-InP samples

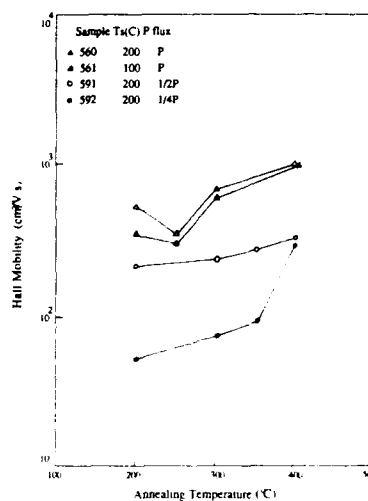


Fig.4 Hall mobility vs annealing temperature of LT-InP samples.

are small compared to that of a virgin InP wafer. Single crystal X-ray diffraction curves taken after annealing above 400°C showed no (111) diffraction peak. The above observation suggests that there is a crystallization (from poly to single crystal or larger polycrystal) process due to the annealing. The satellite peak observed is related to the larger lattice constant in the MBE InP layer which may be due to the excess P. The similar annealing behavior had been observed in LT-GaAs. The reduction of LT-GaAs lattice constant with annealing was explained by the formation of As precipitates. It is speculated that excess P may also form precipitates. Fig.3 and Fig.4 show the resistivity and mobility as a function of annealing temperature for LT-InP layers. The resistivity decreased with annealing while the mobility increased with annealing which is consistent with the improvement of structural quality. The reduction of P_2 flux apparently further deteriorates the LT-InP layer quality which may be related to a low P/In ratio[9].

DISCUSSION

It is interesting to make a comparison between LT-GaAs and LT-InP. It has been shown that, in a 5 μm thick LT-GaAs layer with 1.5 at% excess As, conduction is dominated by the hopping process [10, 11]. The 600°C anneal turns the LT-GaAs into a highly resistive state due to the formation of As precipitates [12] or deep As_{Ga} defect levels [11]. In LT-InP layers, the mobility data indicated a defect-controlled electron transport, which could be related to grain boundaries or to large amounts of isolated defects and disordered regions. The higher temperature annealing did not lead to any increase in resistivity in contrast with LT-GaAs. The excess P may precipitate out under certain condition. However, it is uncertain if the annealing would lead to the formation of large P

precipitates because elemental P solid has a low melting point and a high vapor pressure. Even if P precipitates do exist, the non-metallic properties of P may make its effect insignificant. The carrier concentration ($N_d \sim 7 \times 10^{15}/\text{cm}^3$) in LT-InP after 400°C RTA annealing is on the same order as the shallow impurity density in MBE InP grown at normal substrate temperatures, suggesting that there are low density compensation centers in LT-InP. As in LT-GaAs, a large amount of P_{In} antisite defects may be present in LT-InP. A deep level at $E_c - 0.64\text{eV}$ in InP was reported to be associated with one of the transitions in charge states of P_{In} antisite defect [13]. However the Fermi level position in LT-InP is controlled by shallow levels which may be related to P interstitials P_i , other charge state of P_{In} defects, or some shallow impurities. Any further discussion on the feasibility of utilizing P_{In} defects to achieve high resistive InP has to be based on a more accurate understanding of this defect. Although LT-InP has not yet shown properties similar to LT-GaAs, the good crystalline quality of the LT-InP layer may still be of interest since the low growth temperature has advantages in reduction of interface roughness and segregation of undesirable impurities into the epilayer [14].

CONCLUSION

The InP layers grown by MBE at low substrate temperature (200°C and 100°C) are polycrystal with over 7at% excess P for sample grown with normal P_2 flux. Crystal quality are improved by RTA annealing. However, the resistivity decreased from 60 Ωcm in as-grown sample (# 561) to 0.82 Ωcm in 400°C annealed sample. The low melting point, high vapor pressure and non-metallic nature of P solid, and the low density compensation centers may all contribute to the low resistivity of LT-InP.

ACKNOWLEDGEMENTS

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GROWTH AND CHARACTERIZATION OF LOW TEMPERATURE InP BY GAS SOURCE MBE

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The introduction of GaAs grown at low MBE growth temperatures has spurred considerable activity in attempts to understand conduction mechanisms and optical properties. In LT GaAs, the formation of microscopic As precipitates dominates the conductivity, producing electronic transport mainly by variable range hopping conduction. The resulting high resistivity and short carrier lifetimes have enabled the use of LT GaAs in FET buffer layers as well as in ultra-fast optical switches. An extension to AlInAs has also been performed and it was seen that variable range hopping is also present in the As-based ternary.

We report the optical and electronic properties of InP grown at low temperatures in a gas source MBE using dimeric phosphorus produced from cracked phosphine. The conductivity is higher than the equivalent GaAs LT material and does not have the same temperature dependence. The conditions under which growth occurs i.e., substrate temperatures, V/III ratios and annealing is explored. The structural properties, temperature dependence of the conductivity, deep level structure and the photoluminescence properties of the material are also investigated.

Introduction

The application of MBE GaAs grown at temperatures below 300°C as an electrical buffer layer in field effect transistors [1] has spurred an investigation of other materials grown at low temperatures. Other material systems grown at low temperatures are AlGaAs [2] and InAlAs [3]. Several applications of low temperature (LT) materials have been developed in electronic and photonic devices. In this paper, we report the growth of InP at low temperatures by gas source MBE using sources of solid indium and P₂. The dependence of electrical and optical measurements are explored as a function of growth temperature and V/III ratio. The as-grown material properties are also measured as a function of anneal time and a correlation with phosphorus precipitates and ordered microcrystals observed by transmission electron microscopy (TEM) is made.

Growth of LT InP

Epitaxial layers were grown in a VG V80-H MBE system with solid indium and cracked phosphine. Two sets of samples were grown on semi insulating, Fe doped InP substrates for this study. The first and second sets had epitaxial layer thicknesses of 1.5 µm and 0.3µm respectively. This was done to obtain material above and below the critical thickness for crystalline growth which is determined by the crystal strain induced by the excess P incorporated at low temperatures. Growth temperatures of 240°C, 280°C and 320°C at a V/III atomic ratio of 1.15 were used for the growth temperature dependence study. Samples grown at 240°C at V/III atomic ratios of 1.65, 1.50 and 1.25 were used for the V/III ratio dependence study. The V/III atomic ratios were measured by RHEED oscillations at the normal InP growth temperature of 495°C. A growth rate of 0.6µm/hr was used. Temperatures above 400°C were monitored using an optical pyrometer. For temperatures below 400°C, the system thermocouple temperature was calibrated against the melting points of indium and tin.

The oxide was desorbed at 500°C and the substrate annealed at 520°C for 10 minutes under a P₂ flux before growth of the LT layers. P₂ was generated by cracking of phosphine at 1000°C in a high pressure cracker [4].

The reflection high energy electron diffraction (RHEED) pattern begins as a standard 2X4 and turns spotty during LT InP growth. At the end of growth, the pattern is diffuse. A 500°C anneal step is then performed to promote precipitate formation as in the LT GaAs process. The anneal was performed under a P₂ flux by ramping from the growth temperature to the anneal temperature of 500°C in five minutes. During the

500°C anneal sequence a faint 2X4 pattern improves into a clearly defined 2X4 pattern similar to the substrate's. Samples that were annealed for 10 minutes and 40 minutes were produced for the anneal time study described below.

Structural properties (TEM)

Cross sectional transmission electron microscopy (TEM) was performed (near 110 zone axis conditions) on several samples which were prepared by mechanical grinding and low angle argon ion milling. The microscope used was an Akashi 002B operating at 200keV. The epitaxial layers having a thickness of 1.5 μ m exhibited a moderate to low dislocation density and thin twin planes on {111} extending approximately 0.5 μ m from the LT layer surface. Accurate determination of the critical thickness as a function of growth parameters was not undertaken in this study. Figure 1 is a TEM diffraction contrast micrograph of the 1.5 μ m LT InP layer grown at 240°C. Throughout the layer, a density of approximately 1×10^{10} precipitates per square centimeter ranging in size from 100Å to 500Å was observed. These were analyzed by electron probe energy dispersive x-ray nanospectroscopy and found to be phosphorus-rich. Moire fringes on the precipitates and microdiffraction showed them to be crystalline. Two types of structures are seen in figure 1. The small, solid precipitates are inside the crystal while the large annular, dark-centered ones are predominantly on the surface. The latter morphology is an artifact from sample preparation. The precipitate density is a factor of ten less than that observed for As precipitates in LT GaAs. The average small precipitate size is 250Å which is more than twice the average size found for As precipitates grown by As₂ [5].



Figure 1 Transmission electron micrograph at 100,000 magnification shows the phosphorus-rich precipitates in the single crystal region of the LT InP epitaxial layer.

Electrical and optical properties

Test samples for Hall effect measurements were fabricated by alloying indium dots onto 0.75cmX0.75cm pieces of material. The samples were then mounted in a Helitran cryostat in which the temperature was varied from 10K to 300K for the temperature dependent Hall measurements. Photoluminescence measurements were made in a Janis Supravertemp cryostat. The samples were optically excited with the 496.5 nm line of an argon ion laser. Excitation power densities used were approximately 100 mW/cm² and spectra were recorded by photon counting techniques through a 0.75 meter spectrometer.

Figure 2 shows the carrier concentration and resistivity of three 0.3 μm thick samples grown at the three different substrate temperatures (T_s). Samples having thicknesses of 1.5 μm were very conductive and exhibited resistivities on the order of $10^{-2} \Omega\text{-cm}$ with electron concentrations in the mid 10^{17}cm^{-3} range and are not included in this figure.

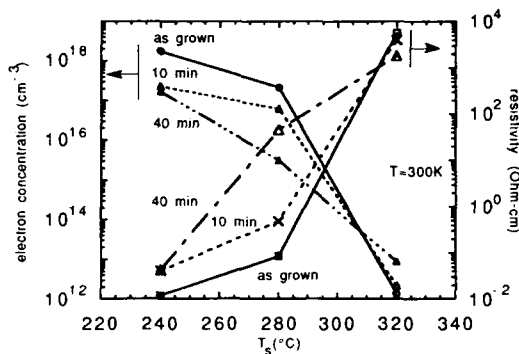


Figure 2 Carrier concentration and resistivity of three samples grown at different substrate temperatures.

grown at very high V/III flux ratios. It is observed that under these conditions, the highest resistivity is less than that found in LT GaAs (typically $>10^6 \Omega\text{-cm}$). The electron mobility was seen to increase from 300 to 400 cm^2/Vsec over this growth temperature range.

In the series grown at $T_s=240^\circ\text{C}$ with varying V/III ratio, the mobility is seen to increase as a function of decreasing V/III ratio from 200 cm^2/Vsec to 675 cm^2/Vsec (compare with the SI InP substrate mobility of $\sim 2900 \text{ cm}^2/\text{Vsec}$). There is a corresponding change in resistivity from 0.19 $\Omega\text{-cm}$ to 0.04 $\Omega\text{-cm}$. The resistivity of the InP:Fe substrate was over 10^3 times higher than any of the epitaxial layers at all temperatures so the Hall measurements represent properties of the LT layers.

An investigation of conduction mechanisms in the LT InP was warranted after the observation of P precipitates to obtain more insight into the issue of the role of precipitates on LT material conduction. To this end, 3 mm wide, parallel indium contacts were alloyed to the films to make ohmic contacts and the current versus temperature monitored. Figure 3 shows the calculated conductivity of the different layers as a function of temperature.

The conductivity of the SI InP substrate is below the detection limit of our measurement below approximately 230K, above this the deep compensating trap level (Fe) begins to ionize by thermionic emission with its thermal activation energy of 0.67eV. A similar behavior is observed in the LT InP layer grown at 320°C which shows an activation energy of 0.61eV. The current begins to increase approximately thirty degrees lower in this sample indicating that shallower traps are present, contributing to the conduction. The samples grown at 240°C and 280°C show high conductivity down to approximately 10K and could not be described by a thermionic emission model. Below 10K an apparent freeze out of carriers is probably due to a shallow defect level. As in the case of LT GaAs [7,8], the conductivity follows a functional form of $\ln(\sigma) \sim T^{-\nu}$ (with $\nu = 0.25$) indicating that variable range hopping conduction is dominating at low temperatures. A difference between the InP and GaAs samples is that the range of temperatures that hopping conduction occurs is smaller in InP probably because the precipitate density is lower. Hopping can either occur among deep trap states or between P precipitates. The average distance between precipitates was measured by TEM to be 1000Å and is thus too large to produce appreciable hopping current in these samples. Hopping conduction

The electron concentration in the 0.3 μm thick samples decreases from low 10^{18} cm^{-3} at $T_s = 240^\circ\text{C}$ to $1 \times 10^{12} \text{ cm}^{-3}$ (depleted) at $T_s = 320^\circ\text{C}$ while the resistivity changes from $10^{-2} \Omega\text{-cm}$ to almost $10^4 \Omega\text{-cm}$ over the same temperature range. The large change in carrier concentration at approximately 350°C is consistent with that observed in previous work on InP grown at low temperatures [6] although in that work the lowest carrier concentration was mid 10^{16} cm^{-3} and all samples were

behavior was not observed in the SI InP substrate nor in the 320°C LT InP epitaxial layer because the conductivity is out of the range of our measurement equipment at the low temperatures.

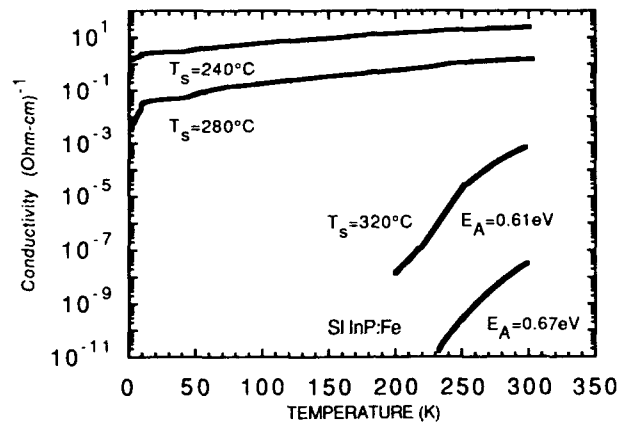


Figure 3 Conductivity versus temperature for a semi insulating InP substrate and GSMBE LT InP epitaxial layers. The two low temperature growths exhibit variable range hopping behavior absent in the 320°C sample and substrate. At high temperatures, conduction in the latter two samples is by thermionic emission from deep traps.

Annealing of LT GaAs is required to obtain the high resistivity from the low resistivity as-grown material. Attempts to understand the annealing mechanisms in LT InP by photoluminescence (PL) are described here. All spectra within each figure were obtained under identical excitation conditions, slit widths and photomultiplier tube bias for comparison purposes. Figure 4 shows the PL spectra of the three unannealed (as-grown) samples whose electrical properties are shown in figure 2.

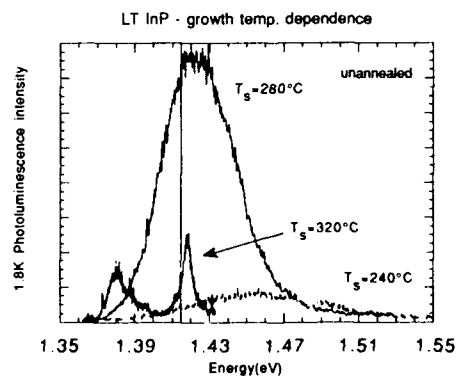


Figure 4 Photoluminescence of LT InP as a function of growth temperature, T_s , from 240°C to 320°C.

A vertical line has been provided at the normal (bulk) InP band edge energy (at 1.8K) of 1.415 eV to aid in comparing the different spectra. At 240°C a broad luminescence (FWHM ~85meV) is observed at 1.45 eV which is greater than the InP bandgap. This is due to strain introduced by the excess P in the lattice which increases the bandgap. This behavior was also observed in as-grown LT GaAs[9].

The 280°C sample PL peak energy (1.425 eV) is shifted toward, but still above, the bulk InP band edge and the line width decreases to 48meV. The shoulders suggest regions of locally high strain as they are on the high energy side of the peak. At 320°C the band edge peak energy is 1.418 eV with a linewidth of 6 meV indicating very little strain in the epitaxial layer. A second band consisting of approximately four peaks is seen around 1.38 eV. These peaks have been attributed [10] to band-to-acceptor (B-A^o) and donor-to-acceptor (D^o-A^o) transitions due to Ca and Mg impurities or carbon [11]. These transitions may not be apparent in the lower temperature samples because of the presence of other nonradiative centers.

Annealing the T_s= 240°C LT InP layer at 500°C for different times produced the PL data in figure 5. Again, the vertical line at the bulk InP band edge energy of

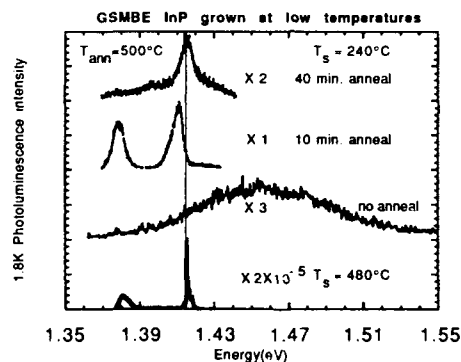


Figure 5 Photoluminescence spectra of the 0.3μm thick LT InP layer grown at 240°C. The bottom curve is the spectrum of an InP layer grown at 480°C for comparison. The luminescence intensities are referenced to the 10 min. annealed sample.

1.415 eV is shown as an aid to the eye. The bottom curve shows the spectrum of an MBE InP layer grown at a normal InP growth temperature of 480°C for reference. Four clearly resolved excitons are seen, with the main one having a FWHM of 0.6 meV. The low energy peak is similar to the one just discussed except that the transitions on the high energy side of 1.380 eV are stronger. The as-grown LT InP layer spectrum is the same broad, single peak as in figure 4. After a 10 minute anneal, the band edge luminescence narrows to 6meV with an energy (1.411 eV) lower than the bulk InP value. The transitions in the 1.38 eV band are now stronger on the low energy side. The low energy peaks are greatly reduced in intensity after the 40 minute anneal and the main peak widens to 8meV and shifts to the bulk InP energy of 1.415 eV. There is a second peak just above the main one which broadens the luminescence line. This may be caused by the appearance of small regions of high strain.

Discussion and conclusions

It was found that the highest resistivity LT InP layers were obtained at a growth temperature of 320°C with a V/III atomic percent of 1.15. The resistivity of the as-grown material increased with annealing at 500°C under a P₂ flux. This behavior was explored by photoluminescence which correlated with the electrical measurements in that the

highest resistivity was obtained at the anneal time of 10 minutes which also produced the narrowest PL linewidth. Annealing for longer than 10 minutes produced lower PL intensities and wider linewidths.

It was also shown that InP grown at low temperatures by gas source MBE and annealed contains crystalline phosphorus-rich precipitates with an average size of 250Å and a density of $1 \times 10^{10} \text{ cm}^{-3}$. This is a lower concentration of precipitates than found in LT GaAs. Thus if the model in which high resistivity is caused due to complete semiconductor depletion by metallic precipitates [12] is valid, then we may not necessarily have complete depletion at the P precipitate densities in the samples studied here. However, variable range hopping conduction is observed in this material at low temperatures (albeit in a narrower temperature range than in LT GaAs) which might indicate certain regions are more fully depleted than others. The remaining conductivity is probably due to shallow and deep levels in the undepleted regions. From the large precipitate size, it could be speculated that there is a large amount of local strain in the crystal which can generate dislocations which may cause high conductivity.

In conclusion, behavior similar to that obtained in the As based semiconductors was observed in the P based III-V semiconductors system. The kinetics of P based MBE growth must be further studied to determine whether an association reaction, similar to that observed for As_2 based growth, causes an increase in the incorporation of excess P at low growth temperatures. The full range of growth parameters still needs to be investigated in more detail for application to particular devices.

Acknowledgement

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STRUCTURAL AND DEFECT STUDY OF LOW TEMPERATURE INP GROWN BY GAS SOURCE MOLECULAR BEAM EPITAXY

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ABSTRACT

The low temperature growth procedure used in the case of GaAs to introduce high concentrations of deep traps such as arsenic antisite defects has been extended to the growth of InP by gas source molecular beam epitaxy. The low temperature growth of InP induces a strong group V stoichiometric deviation (of the order of +1%). On the other hand, Secondary Ion Mass Spectrometry reveals high levels of hydrogen ranging from 3.10^{18} to 3.10^{19} cm⁻³ depending on growth temperature. Undoped layers are found to be resistive without any post annealing. Annealing experiments above 250°C lead to conductive layers suggesting a passivation effect of both shallow donors and acceptors by hydrogen.

INTRODUCTION

The route to produce semi-insulating (SI) III-V materials is based on the introduction of a concentration of deep traps larger than the residual shallow impurity concentration. That can be obtained by a low temperature growth process. GaAs epitaxial layers grown by Molecular Beam Epitaxy (MBE) at low temperature (200°C-300°C) have shown interesting SI properties [1,2]. The deep traps have been correlated with the strong As-rich stoichiometry (up to 1%) and identified as arsenic antisite defects [3]. This type of material has been used as buffer layers to reduce backgating, sidegating and light sensitivity effects in MESFET [4, 5]. This low temperature growth approach used successfully for GaAs can be extended to other arsenide compounds such as AlGaAs [6], AlInAs [7]. Concerning InP, the growth of SI layers is usually obtained by iron doping. However, the Fe dopant gives rise to various problems such as low thermal stability, electrical activity which decreases sharply on vicinal (100) and high index planes (111) and

finally dopant interactions when co-doped with Zn [8]. Anionic antisite (P_{In}) could also, in principle, play a decisive role in the production of SI layers by Fermi level pinning since, by analogy with the As_{Ga} , the phosphorus antisite is a double donor with a first ionisation level 0/+ located near midgap. However, it appears difficult to grow InP at low temperature by the MOVPE technique because the growth is limited to 300-350°C by the surface decomposition of both metalorganic and hydrides molecules. A well adapted growth technique seems to be the so called Gas Source MBE (GSMBE) which uses a solid In source and precracked PH_3 . The absence of a decomposition limiting process at the growing surface allows the use of substrate temperatures as low as room temperature. In this communication we will concentrate on the structural and defect analysis of InP layers grown at low temperature (LT) by GSMBE.

EXPERIMENTAL GROWTH DETAILS

The growth has been carried out in a CBE Riber 32P machine where an In solid source has been installed. PH_3 is introduced via a low pressure Molybdenum cracker cell achieving a complete PH_3 dissociation into P_2 at 800°C. The substrate temperature was calibrated using the melting point of InSb and then controlled by a thermocouple positionned on the backside of the substrate holder. InP growth rate and PH_3 flow rate were fixed to 1 μ m/h and 20sccm respectively for all experiments. Typical growth chamber pressures are around 9×10^{-5} Torr. Lowering the temperature to 200°C under PH_3 flux leads to a change of the reflection high energy electron diffraction (RHEED) pattern from a 2X4 to a 2X1 reconstruction. When growth is initiated, the surface reconstruction shifts to a 1X1. Film composition is determined by electron microprobe analysis.

RESULTS

All the samples grown exhibit a mirror-like aspect even when the layers are amorphous. Figure 1 shows the phosphorus stoichiometry as a function of growth temperature. Lowering growth temperature to 200°C or below leads to an excess phosphorus concentration of at least 1% as in the case of LT GaAs. It is yet not clear how the phosphorus atoms in excess are incorporated but it can be suggested that it is likely as antisites and clusters by analogy with GaAs. The effect of lowering the growth temperature down to 200°C also leads to a

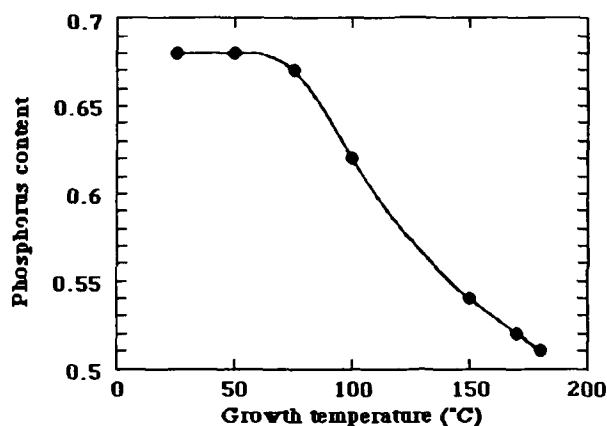


Fig 1: Phosphorus stoichiometry as a function of the growth temperature without post annealing.

reduction of surface reactions and mobilities of the molecules on the surface, thus inducing a transition in the growth mode. As shown in figure 1, we can define three temperature ranges: in the first (170-200°C) monocrystalline layers are produced; the second (100-170°C) produces polycrystalline layers and finally in the third (25-100°C) the layers are amorphous. It should be noted that a recrystallisation of the amorphous layers is possible by an annealing step at 600°C after the low temperature growth, on top of which epitaxial growth can be made. It appears thus that the temperature range of interest is 170-200°C, at least under the growth conditions used in this study.

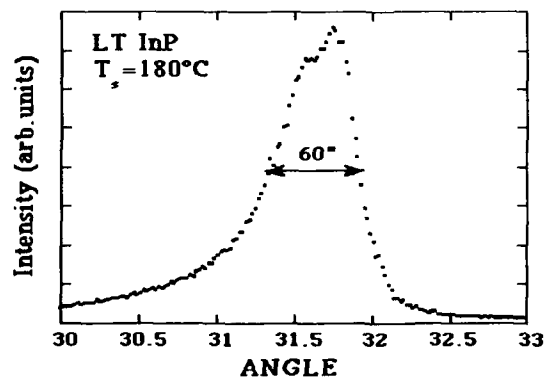


Fig 2: 400 X-ray diffraction of an InP layer grown at 180°C

Figure 2 shows the (400) double X-ray diffraction spectrum of a 2 μ m thick unannealed InP layer grown at 180°C. Two components can be clearly observed in the diffraction peak. The full width at half maximum is low (60") demonstrating the good crystalline quality of the layer. The lattice constant difference of the layer from that of the substrate can be attributed to the presence of strain induced by the phosphorus excess. After high temperature annealing (560°C), the rocking curve of the epilayer is quite similar, if not identical to that of the substrate suggesting that phosphorus has migrated, thereby reducing the net strain in the layer. Impurity analysis by Secondary Ion Mass Spectrometry (SIMS) provides interesting features. The main residual impurities and related concentrations are compiled in the Table 1 and compared to those obtained when the growth is carried out at high temperatures (530°C). Carbon is the main impurity. It acts mainly as a shallow donor in InP [9] contrary to GaAs where it is

Elements	T _s =180°C	T _s =530°C
[H]	3.10 ¹⁸	5.10 ¹⁶
[O]	10 ¹⁷	8.10 ¹⁶
[C]	5.10 ¹⁶	5.10 ¹⁵
[Si]+[S]	5.10 ¹⁵	10 ¹⁵

Table 1: Residual impurities concentration in InP grown at low and high temperature layers.

incorporated as acceptor in As sites. When compared with residual impurities found in conventional growth InP (530°C), the main feature of the LT growth is the high level of hydrogen (3x10¹⁸ cm⁻³) incorporated in the layers. Typical hydrogen concentrations in InP grown at 530°C are in the range of 5x10¹⁶ to 1x10¹⁷ cm⁻³. Hydrogen levels up to 4x10¹⁹cm⁻³ are measured in the amorphous and polycrystalline samples grown at the lowest temperatures. This hydrogen comes from the thermal dissociation of PH₃ into P₂ and H₂. The higher carbon concentration determined in the LT growth is due to the current use of metal-organic group III sources in our growth system which leads to a relatively high carbon uptake.

The role of hydrogen in crystalline semiconductors has been observed to change the electrical and optical properties of the layers. Hydrogen has been found to form neutral complexes and to passivate dopant atoms, and eventually other impurities and lattice defects [11]. However little information is available, to our knowledge concerning InP grown in a

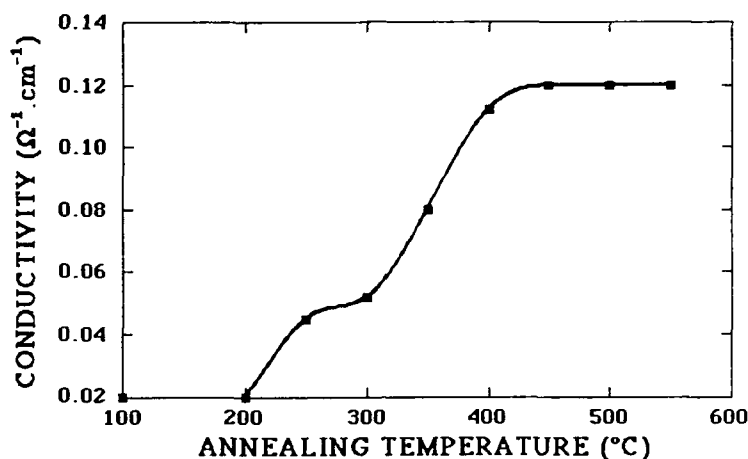


Fig 3: InP conductivity variation with annealing temperature

hydrogen environment as it is the case in GSMBE. All the annealed layers are found to be n-type at 300K with carrier concentrations in the range of 10^{16} cm^{-3} with very low associated mobilities ranging from 400 to $900 \text{ cm}^2/\text{V/s}$. Conductivity has been examined versus thermal annealing in the 100°C - 500°C temperature range. Figure 3 shows the conductivity as a function of the temperature. At temperatures lower than 200°C all the samples exhibit a relatively high resistivity (5×10^2 - $10^3 \text{ } \Omega \cdot \text{cm}$). The conductivity increases with increasing the annealing temperature until it reaches, around 450°C , a constant value. A reasonable explanation for this behavior is that shallow donor and/or acceptors passivated by hydrogen become electrically active following H out-diffusion. This result is in good agreement with infrared absorption measurements on Hydrogen complexes in bulk InP [11]. Nevertheless, other possibilities have to be considered such as annealing of defects which compensate the shallow donors or the incorporation on substitutional sites of the shallow impurities.

CONCLUSION

The LT growth of InP by GSMBE is found to introduce an excess of phosphorus atoms. Good quality single crystals can be obtained with P

excess at least of 1% in the 170-200°C temperature range. Without any post annealing the samples exhibit a relatively high resistivity (5×10^2 - $10^3 \Omega \cdot \text{cm}$). The introduction of a post annealing step up to 250°C leads to conductive layers with a net electron concentration of about 10^{16} cm^{-3} having low mobilities. Although P_{In} defects are introduced by the low temperature growth, all the layers are found to be n-type. It is necessary in order to obtain SI InP, that acceptor-type defects with large ionisation energies are created to compensate the remaining donors. It is possible to achieve this by doping with a p-type impurity such as beryllium. Using this approach, preliminary measurements on Be doped LT InP have given high resistivities above $10^5 \Omega \cdot \text{cm}$ at room temperature after a post-annealing.

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LOW-TEMPERATURE GROWTH AND CHARACTERIZATION OF InP GROWN BY GAS-SOURCE MOLECULAR-BEAM EPITAXY

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ABSTRACT

Low-temperature (LT) growth of InP by gas-source molecular-beam epitaxy has been studied. Contrary to GaAs, InP grown at low temperature (from 200 °C to 410 °C) shows n-type, low-resistivity properties. The electron concentration changes dramatically with growth temperature. A model of P antisite defects formed during LT growth was used to explain this experimental result. Ex-situ annealing can increase the resistivity, but only by a factor of about 6. Heavily Be-doped LT InP also shows n-type property. We believe this is the first report of an extremely high concentration of donors formed in LT InP and n-type doping by Be in III-V compounds.

INTRODUCTION

Annealed GaAs layers grown at low temperature exhibit extremely high resistivity [1-3] and short carrier lifetime [4, 5], but unexpectedly high mobility [4]. High resistivity is desirable for both field-effect transistors and optoelectronic devices. Short carrier lifetime combined with high mobility, is advantageous for ultra-fast switches. Low-temperature growth of various arsenides has become one of the most interesting topics today. Different models have been proposed to explain the properties of LT GaAs [6, 7].

As another important member of the III-V family, InP grown at low temperature and its properties have not been investigated. In this paper, we have systematically studied the growth of InP by gas-source molecular-beam epitaxy (GSMBE) at low temperature (from 200°C to 410°C), and the properties of both as-grown and annealed LT InP thin films by reflection high-energy electron diffraction (RHEED), Hall-effect measurement, I-V characteristics, and photoluminescence. Extremely high concentration of donors and anomalous doping behavior of Be in LT InP grown by GSMBE has been observed for the first time.

EXPERIMENTAL PROCEDURE

The samples were grown in an Intervac (Varian) Gen-II MBE machine modified to handle arsine and phosphine. An Intervac gas cracker for cracking group-V hydrides and EPI

effusion cells for In, Ga, Be and Al were used. The growth rate of InP was fixed at 1 monolayer per second. The growth temperature was calibrated by a pyrometer and the melting point of InSb. The cracker temperature was 1000°C. The LT InP layers were grown in the growth temperature range of 200°C to 410°C, and with a phosphine flow rate range of 0.8 sccm to 2.4 sccm. Ex-situ annealing was performed in forming gas (15% H_2 and 85% N_2). During proximity annealing, the sample surface was protected by another piece of InP substrate. RHEED pattern was used to monitor the growth front. Hall-effect measurements and I-V curves were used to characterize electrical properties of LT InP grown on (001) semi-insulating and n^+ -InP substrates, respectively. Photoluminescence was used to characterize optical properties of LT InP.

RESULTS AND DISCUSSION

Among growth parameters, the growth temperature is the most important. Figure 1 shows the electron concentration of undoped InP as a function of growth temperature at a phosphine flow rate of 1.5 sccm. Below 500°C, the electron concentration of undoped InP,

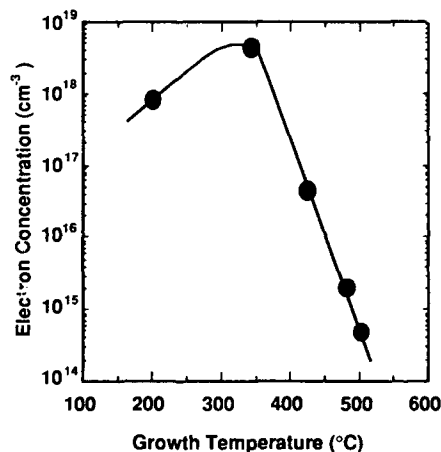


Fig.1 The electron concentration of GSMBE InP vs. growth temperature at 1.5 sccm of phosphine flow rate and 1.0 monolayer per second of growth rate.

similar to InAs [8], increases with decreasing growth temperature. At 340°C, the electron concentration is as high as $4.5 \times 10^{18} \text{ cm}^{-3}$. When the growth temperature decreases further, the electron concentration begins to decrease. We believe that native defects dominate electrical properties of LT InP. At a fixed phosphine flow rate, the lower the growth temperature is, the higher the phosphorus incorporation into the layer. The species of native defects in InP are P_i (phosphorus self-interstitial), P_{In} (phosphorus antisite defect), In_i (In self-interstitial), In_P (In antisite defect) and V_P (phosphorus vacancy) for In-rich InP; or combination of these defects. Of

these, P_{In} , In_i and V_P are donors, and the others are acceptors. Because phosphorus atoms are much smaller than In atoms, it is expected that more P atoms will occupy the In sites, instead of interstitial sites. This can then explain that undoped LT InP is n-type. However, when the growth temperature decreases further, more P_i may be present because many extra phosphorus atoms become incorporated into the deposited layer. Therefore, the electron concentration decreases. Photoluminescence measurements at 40 K show that the full width at half maximum (FWHM) is 2 meV for a sample grown at 500 °C, 11 meV for a sample grown at 410 °C, and no luminescence for samples grown at temperatures below 400 °C.

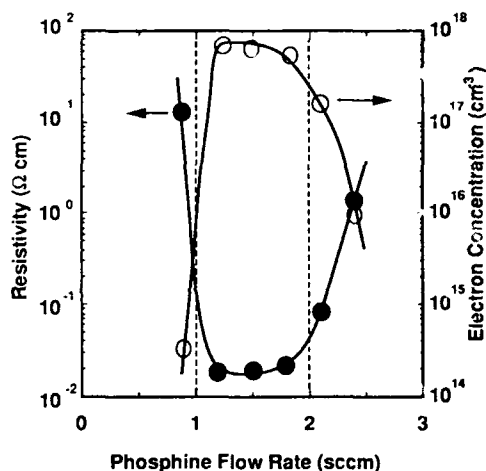


Fig.2 The resistivity (solid circles) and electron concentration (open circles) of LT InP (200°C) vs phosphine flow rate. Growth temperature was 200°C and growth rate was 1.0 monolayer per second. The deposited layers were polycrystalline-like InP if phosphine flow rate below 1.0 sccm or above 2.0 sccm.

Figure 2 shows the resistivity and carrier concentration of undoped LT InP as a function of phosphine flow rate at a growth temperature of 200°C. Between 1.0 sccm and 2.0 sccm of the phosphine flow rate, the electron concentration of undoped LT InP is about $7 \times 10^{17} \text{ cm}^{-3}$ with a resistivity about 0.02 Ω-cm. Mirror-like surface morphology of these samples were obtained. On the other hand, if the phosphine flow rate is below 1.0 sccm or above 2.0 sccm, LT InP grown at 200°C is polycrystalline according to the RHEED pattern and its resistivity (carrier concentration) increases (decreases) with increasing nonstoichiometry. The surface morphology of these samples becomes either white (In rich) or black (P rich). At a fixed growth

temperature and In-beam flux, the crystallinity and surface morphology of LT InP layers deteriorate with increasing PH_3 flow rate above 1.0 sccm. For the LT InP layer grown on an n^+ -InP substrate, Au dots are evaporated on the surface. I-V curves show very good ohmic contact characteristics between Au and LT InP without any alloying.

Be is a popular p-type dopant for InP grown by molecular-beam epitaxy (MBE) [9]. One can obtain an acceptor concentration as high as $3 \times 10^{19} \text{ cm}^{-3}$. However, as shown in Figure 3, we can not obtain p-type InP by Be-doping in LT InP, even the Be doping level is as high as $1 \times 10^{19} \text{ cm}^{-3}$ of acceptor concentration for normally grown InP in our system. With increasing

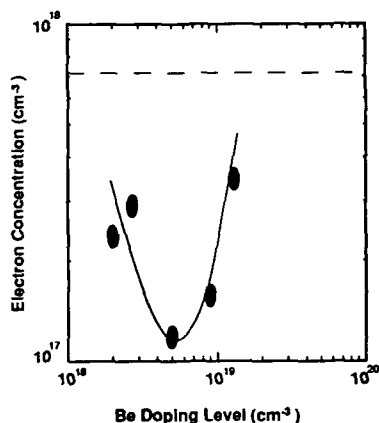


Fig.3 The electron concentration of Be-doped LT InP vs Be doping level. The dashed line shows the electron concentration of undoped LT InP. Growth temperature was 200°C. Phosphine flow rate was 1.5 sccm.

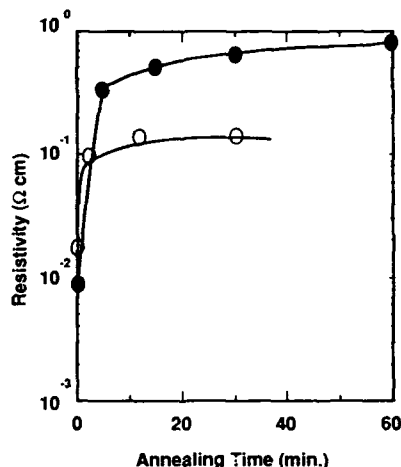


Fig.4 The resistivity of undoped (open circles) and Be-doped (solid circles, Be-850°C) LT InP vs ex-situ annealing time (in forming gas). Anneal temperature was 500°C.

Be doping level the electron concentration in LT InP decreases first and then increases. We believe that there must be some interaction between native defects and Be atoms. Because Be is a group-II element, the only possibility for Be being a donor in InP is that it is self-interstitial. Therefore, in LT InP, if the Be doping level is not too high ($< 5 \times 10^{18} \text{ cm}^{-3}$), a fraction of the Be atoms still occupy In sites as acceptors. When the Be doping level is high ($> 5 \times 10^{18} \text{ cm}^{-3}$), more Be atoms may prefer to occupy interstitial sites and form $(\text{Be}_{\text{In}}-\text{Be}_i)$ complex, which has been taken as a deep donor [10]. *Ex-situ* annealing at 500°C for 30 minutes in forming gas can increase the resistivity of undoped and Be-doped LT InP by factors of 6 and 60, respectively, as shown in Figure 4. Part of the initial increase in resistivity upon annealing may be due to reactivation of impurities and defects that have been passivated by hydrogen which comes from cracked phosphine.

The presence of hydrogen during growth is an important difference between GSMBE and MBE. Hydrogenation of defects and impurities in III-V compounds has been studied by several groups [11-15]. In GSMBE, at a relatively high, normal growth temperature, hydrogen species from cracked group-V hydrides are not incorporated in the deposited layer. However, hydrogen passivation of defects and dopants may occur during LT growth. At low growth temperature, hydrogen is able to be incorporated into the deposit layer and may passivate some defects and dopants. To investigate this possibility, we grew Si-doped and Be-doped InP layers on (001) semi-insulating InP substrates at a normal growth temperature of 500°C. Then, the sample

temperature was decreased to about 200°C while the layer was exposed to the cracked-phosphine beam for 30 minutes. The cracker temperature was kept at 1000°C. For Be-doped InP, the carrier concentration decreased from $3.5 \times 10^{17} \text{ cm}^{-3}$ to $2.3 \times 10^{17} \text{ cm}^{-3}$, but for Si-doped InP, the carrier concentration remained the same. A similar behavior has been reported in ref. [15] with p^+ -InP:Zn using hydrogen plasma. Compared to the result in ref. [15], hydrogenation of Be is not as effective as that of Zn. The difference may result from different elements or different hydrogen source. Therefore, the hydrogen presence during GSMBE can affect the properties of deposited layers, especially for LT grown materials. Even though we could not distinguish how much of the resistivity change come from dehydrogenation of native defects and/or impurities in Figure 4 at this time, hydrogenation of defects and impurities during LT GSMBE, we believe, is one of the most important factors that dominate the property of LT grown materials. Further studies on the effect of hydrogen on the deposited layer properties is being performed in this group.

CONCLUSION

The properties of LT InP have been studied systematically. Contrary to GaAs, LT InP shows n-type, low resistivity. Be in LT InP exhibits abnormal doping behavior. P-type LT InP:Be can not be obtained. Be interstitial has been assumed to explain this anomalous experimental result.

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TEM AND HREM STUDIES OF AS-GROWN LOW-TEMPERATURE MOLECULAR BEAM EPITAXIAL $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ HETEROLAYERS

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ABSTRACT

Transmission and High Resolution Electron Microscopy have been used to study the dramatic changes in crystalline quality which occur in As-rich $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ layers when the growth temperature is lowered. We have found that for temperatures as low as 200°C and for a flux ratio of 20, the layers can be of high quality. For the lowest growth temperature of 150°C , pyramidal defects as well as hexagonal As grains are found which are characteristic of the breakdown of the monocrystalline growth in these layers. A mechanism for the formation of these defects is proposed based on their crystallographic structure. The fast photo response previously observed in these layers must be related to the presence of these defects.

INTRODUCTION

InAlAs layers grown under low-temperature conditions have been recently used as buffer layers for field-effect transistors, resulting in improved device performance [1]. It has previously been shown [2] that recombination times as low as 400 fs could be obtained for InAlAs grown at a temperature as low as 150°C . This material therefore shows great potential for the realization of subpicosecond optoelectronic switches and other applications. There are striking similarities between this material and the more well studied "low-temperature" GaAs. Both materials are generally grown at low temperature (in the $150\text{--}300^\circ\text{C}$ range) under arsenic overpressure and thereafter exhibit semi-insulating properties and fast response [3]. We have shown in a previous paper that the stoichiometry of the layers as measured by particle induced x-ray emission (PIXE) experiments is a strong function of growth temperature [4]. It was found that, as in the case of LT GaAs, the semi-insulating properties of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ layers are related to the presence of a large fraction of excess As in these layers, up to several percent. The content of excess As (1-2%) in the layers is increased when lowering the growth temperature ($<200^\circ\text{C}$).

Since it is likely that a device is to be fabricated on an epi-layer grown on top of such a layer, the crystalline quality of these layers is of great importance. For "low-temperature" (LT) GaAs and InAlAs , however, the range of growth conditions for which good crystallinity, good semi-insulating properties and fast response are simultaneously obtained is quite narrow, if it exists at all.

In this paper we show that the crystalline quality of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ layers is a sensitive function of the growth temperature. Transmission electron microscopy (TEM) in plane view and cross-section as well as High Resolution Electron Microscopy (HREM) were used to study the influence of the growth temperature on the structure of the layers and the "pyramidal defects", which characterize the breakdown of crystalline growth for the lowest growth temperature of 150°C .

EXPERIMENTAL DETAILS

1- μm -thick $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ layers were grown on Fe-doped semi-insulating (100) InP substrates by MBE at a growth rate of 0.7-1 $\mu\text{m/hr}$ and under As overpressure ($\text{As}/(\text{As}+\text{In})$ flux ratio ~ 20) at 150°C, 200°C, 300°C and 480°C. The substrates were prepared for growth by standard degreasing and etching in 0.5% bromine methanol and 5 H_2SO_4 : 1 H_2O : 1 H_2O_2 . Growth was done on As stabilized (2x4) reconstructed surfaces. One sample grown at 150°C was further annealed in situ at 500°C for 10 min. The morphology of the samples was characterized by increased roughness with lowering of growth temperature. High resistivity behavior was observed in all the layers. For the material grown at 150°C, the resistivity further increased by approximately an order of magnitude after annealing [2].

TEM experiments of plane view as well as cross-section samples were carried out on a JEOL 200 keV top entry microscope with a resolution of 0.24 nm and on the ARM of Berkeley operating at 800 keV with a resolution of 0.17 nm.

RESULTS AND DISCUSSION

Fig. 1 is a set of micrographs showing the change in the structure of the layers grown at different temperatures. All layers are characterized by a small lattice mismatch (0.5-1.5%) to the InP substrate as recognized by x-ray diffraction. This lattice mismatch is caused by a slight change of the element ratio (In/As , $x(\text{In}) < 0.52$) up to about 7%, which was measured by PIXE. In all layers stacking faults could be observed with different concentration (450°C: $\approx 10^7\text{cm}^{-2}$, 200°C: $\approx 10^8\text{cm}^{-2}$) starting at some depth from the interface. They extend toward the surface while sometimes forming microtwins. These defects are related to the reduction of the mentioned lattice mismatch. For the sample grown at 300°C a few other defects were also found, such as "hair-pin" and other complicated defects. The layers grown at 200°C contains a high density of stacking faults, which lie on two of the four possible {111} planes, e.g. in the case of a [001] sample on (111) and ($\bar{1}\bar{1}\bar{1}$). On the two other {111} planes (e.g. (111) and ($\bar{1}\bar{1}\bar{1}$)) ordering of the group-III elements occurs (CuPt-type) in small regions. From simulations of electron diffraction patterns [4] it followed that these ordered zones have a substructure of a size of about 1 nm.

For $T_g = 150^\circ\text{C}$, however, the structure of the layer is no longer monocrystalline and "pyramidal" defects are clearly seen in high density. They can be described as a "core" surrounded by two symmetrical "wings". They mostly consist of twin systems associated with dislocations. Electron diffraction and dark field experiments on cross sectional samples clearly show the presence of primary and secondary twins. Fig. 2a is a HREM image showing the structure of a typical "wing" far from the core of the defect. This part of the defect consists of a twin system, i.e., every 4-8 {111} planes there is a stacking fault giving rise to a twin. As this wing comes closer to the core of the defect, the twin systems tend to be associated with many dislocations. This leads to distortions in the crystalline network and to strong bending of the {111} planes as seen in the HREM image of Fig. 2b. This also allows the growth direction to be slightly changed from place to place (from $\langle 100 \rangle$ to the direction of $\langle 221 \rangle$), and this gets worse as the growth proceeds. Dark field imaging using the spots characteristic of secondary twinning shows that the core of a pyramidal defect is mostly composed of grains with both orientations but with many distortions and dislocations. Complete crystallographic details will be given elsewhere [5].

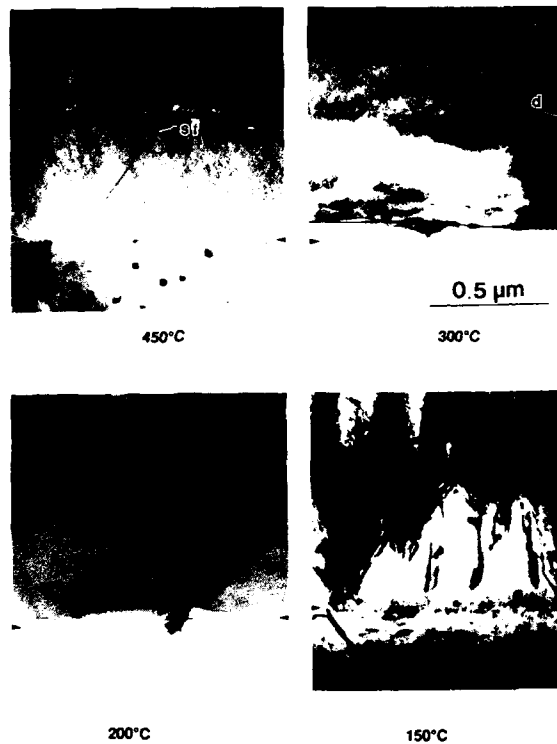


Fig.1 Set of cross-section HREM images showing the structure of the layers grown at different temperatures. Notice the "pyramidal defects" at $T_g=150^\circ\text{C}$.

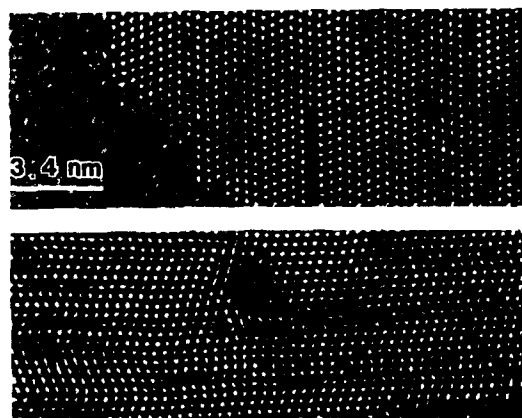


Fig. 2 HREM images of the "wing" part of a pyramidal defect a) far from the core of the defect; b) close to the core.

Fig. 3a is a plane view image obtained from the top of the layer. It shows that the near surface layer consists of different grains of average size about 50 nm. Most of the grains are heavily faulted on their {111} planes. Fig. 3b is a selected area electron diffraction pattern obtained when the electron beam is close to $\langle 100 \rangle$ in the substrate. This pattern may be decomposed as the overlapping of different elemental patterns. The two main contributions are due to the InAlAs material seen near the $\langle 100 \rangle$ and $\langle 011 \rangle$ directions. This is a clear indication that the growth direction of the layer is changed from $\langle 100 \rangle$ to $\langle 011 \rangle$ (also observed in the case of LT GaAs [8]). Moreover, additional spots in the diffraction pattern marked by arrows are readily identified as due to rhombohedral arsenic (often referred to as hexagonal As for crystallographic convenience) having a particular orientation relationship (O.R.) with the InAlAs grains. This O.R. is usually the same as that found for hexagonal precipitates in GaAs [6] although some other O.R.s are also detected.

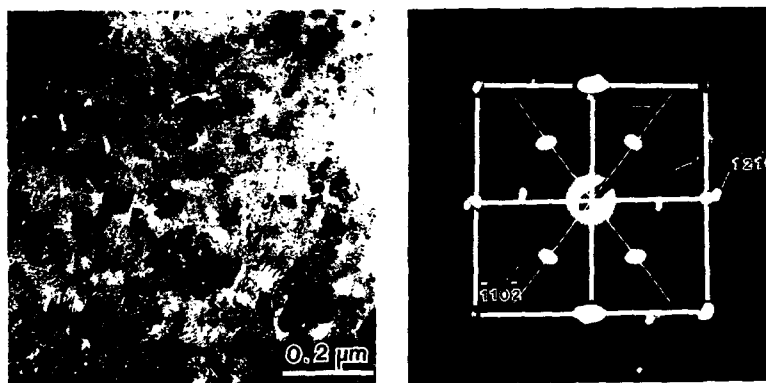


Fig. 3 a) Bright field image of the layer seen from the surface; b) Typical electron diffraction pattern along $\langle 100 \rangle$ in the substrate. Arrows point toward spots of hexagonal As.

HREM clearly shows the presence of a hexagonal structure compatible with As between adjacent InAlAs grains. Fig. 4a is from such an area and shows three distinct zones in that material. In the upper left of the image, the 0.2 nm fringes are characteristic of the InAlAs material seen nearly along its $\langle 100 \rangle$ zone axis. The right part of the image shows the same material but seen along a $\langle 011 \rangle$ direction, i.e., the {111} planes are visible in that case. Note that these planes are heavily twinned with many dislocations. In the center of the micrograph, a different phase is seen while its numerical Fourier transform is shown inset. This allows us to check that this image is consistent with the hexagonal As structure seen along the $\langle 1-213 \rangle$ direction. In this case, there is not a simple O.R. of this grain with respect to the substrate. Especially in the near surface region the InAlAs grains may be highly disoriented with respect to their pure primary and secondary twinning components. In Fig. 4b is shown a filtered image of the structure that enhances the visibility of dislocations within the hexagonal As structure.

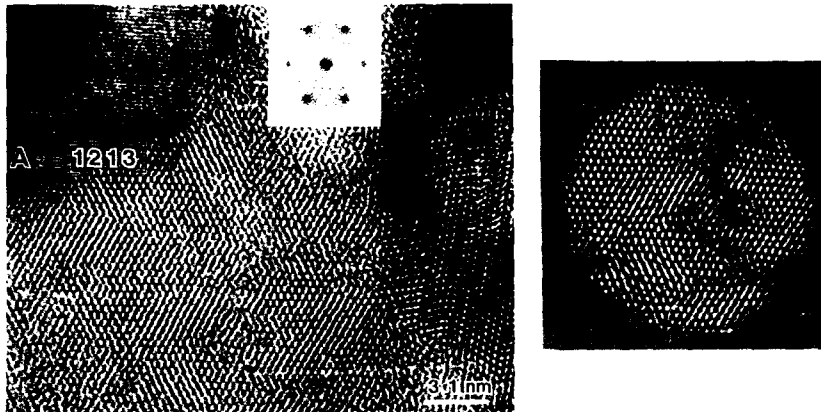


Fig. 4 a) HREM image of hexagonal As grains seen close to the top of the pyramidal defects. Inset are the numerical Fourier transforms of the image. b) Filtered image of the same grain. Note the dislocations within the As structure.

Another proof of the existence of small layers of hexagonal As is given in Fig.5, where a set of fringes characteristic of the (111) planes in InAlAs are seen in the left part of the image. The other structure seen in the center of the image is a hexagonal As structure projected on its basal plane, i.e., exhibiting the 6-fold symmetry. These regions can be correlated to the expected increased incorporation of additional As ($\approx 1-2\%$) in these layers grown at 150°C .

The pyramidal defects have the same morphology as those observed in LT GaAs [7,8]. As already discussed for LT GaAs [9,10] this morphology is formed during growth. This, moreover, has been confirmed by examining annealed samples. Because of the changing In and As content the layers are heavily stressed. The usual stress-relieving mechanism, namely, the creation of dislocations on the surface, which then move down into the layer by glide

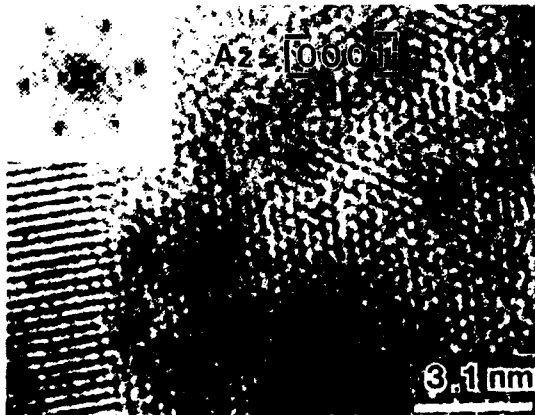


Fig. 5 HREM image of another As grain seen along $\langle 0001 \rangle$. Note the 6-fold symmetry in the corresponding optical diffraction pattern.

mechanisms, cannot operate in this case because of the low growth temperature. Therefore, we assume that the core of a pyramidal defect may grow faster than any other part of the defect or of the substrate. The origin of defect formation is not yet clear; maybe the key to it is the formation of twins in the layer. Since As atoms condense more efficiently on {111} GaAs planes and form hexagonal (0001) planes the surface of the layer near the pyramidal defects becomes rough and {111} facets are developed. This hypothesis is under investigation.

In conclusion, our study shows that 1 μm -thick $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ layers can be grown on InP with a high crystalline quality for $T_g \geq 200^\circ\text{C}$. At a lower growth temperature ($T_g=150^\circ\text{C}$), pyramidal defects are formed which mostly consist of twins, dislocations and small lamella of hexagonal As. A special feature is the occurrence of ordering of group-III elements observed at 200°C , which is likely related to the larger changing of the element ratio. However, for the moment we can not clearly state how much additional As is incorporated in the layers in dependence on T_g . The lower the growth temperature, the higher should be the amount of this excess arsenic that can be incorporated. If this amount is too high, the increase of stress in the layer and also a surface roughening lead to the breakdown of monocrystalline growth. This study also shows that the fast photo response that was previously observed in the layers grown at 150°C [2] is related to either the presence of hexagonal As in the material or, more probably, the large density of defects such as dislocations which are observed in these layers.

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